DISCRETE SEMICONDUCTORS

DATA HANDBOOK

Small- signal Field-effect Transistors

BOOK SC07 1989

Philips Components

PHILIPS

SMALL-SIGNAL FIELD-EFFECT TRANSISTORS

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SELECTION GUIDE

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS	CHARACTERISTICS					remarks	page
		$\pm V_{DS}$	I_G	I_{DSS} min.-max.	$-V_{(P)GS}$ max.	$\lvert y_{fs}\rvert$ min. f = 1 kHz	C_{rs} typ.		
		V	mA	mA	V	mS	pF		
BC264A	TO-92 var.	30	10	2,0-4,5	> 0,5	2,5	1,2	hi-fi amplifiers and a.f. equipment	45
BC264B				3,5-6,5		3,0			45
BC264C				5,0-8,0		3,5			45
BC264D				7,0-12,0		4,0			45
BF245A	TO-92 var.	30	10	2,0-6,5	8,0	3,0-6,5	1,1	d.c., l.f. and h.f. amp.	51
BF245B				6-15					51
BF245C				12-25					51
BF247A	TO-92 var.	25	10	30-80	0,6-14,5	8	3,5	v.h.f. and u.h.f. amp. general purpose sw.	63
BF247B				60-140					63
BF247C				110-250					63
BF256A	TO-92 var.	30	10	3-7	7,5	4,5	0,7	v.h.f. and u.h.f. appl.	65
BF256B				6-13					65
BF256C				11-18					65
BF410A	TO-92 var.	20*	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables	77
BF410B				2,5-7,0	typ. 1,5	4,0		r.f. stages car radios	77
BF410C				6-12	typ. 2,2	6,0		r.f. stages mains radios	77
BF410D				10-18	typ. 3,0	7,0		mixer stages	77
BF510	SOT-23	20	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables	81
BF511				2,5-7,0	typ. 1,5	4,0		r.f. stages car radios	81
BF512				6-12	typ. 2,2	6,0		r.f. stages mains radios	81
BF513				10-18	typ. 3,0	7,0		mixer stages	81
BFR30	SOT-23	25	5	4-10	5	1,0-4,0	0,85	low-level general purpose amplifiers	95
BFR31				1-5	2,5	1,5-4,5			95
BFR101A	SOT-143	30	10	0,2-1,5	1,0	1,2	–	source follower	105
BFR101B				1-5	2,5	2,5	–		105

* Asymmetrical.

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS	CHARACTERISTICS					remarks	page
		$\pm V_{DS}$	I_G	I_{DSS} min.-max.	$-V_{(P)GS}$ max.	$\lvert y_{fs}\rvert$ min. f = 1 kHz	C_{rs} typ.		
		V	mA	mA	V	mS	pF		
BFT46	SOT-23	25	5	0,2-1,5	1,2	1,0	0,85	general purpose ampl.	113
BFW10	TO-72	30	10	8-20	8	3,5-6,5	0,6	broad band up to 300 MHz and differential ampl.	121
BFW11				4-10	6	3,0-6,5			121
BFW12	TO-72	30	5	1-5	2,5	2,0	0,6	low current-low voltage applications	133
BFW13				0,2-1,5	1,2	1,0			133
BFW61	TO-72	25	10	2-20	8	2,0-6,5	$<2,0$	general purpose ampl.	143
2N3822	TO-72	50	10	2-10	6	3,0-6,5	$<3,0$	general purpose h.f. ampl.	185
2N3823	TO-72	30	10	4-20	8	3,5-6,5	$<2,0$	industrial i.f./r.f. ampl.	187

N-channel junction field-effect transistors for differential amplifiers

type	envelope	RATINGS			CHARACTERISTICS							
		individual transistor		total device	individual transistor		total device					
		$\pm V_{DS}$	I_G	I_G	I_{DSS}	$-V_{(P)GS}$	$\lvert \Delta V_{GS} \rvert$	$\lvert \frac{d\Delta V_{GS}}{dT} \rvert$	$\lvert \Delta \frac{1}{g_{fs}} \rvert$	$\lvert \Delta \frac{g_{os}}{g_{fs}} \rvert$	CMRR	page
		V	mA	mA	min. max. mA	min. max. V	max. mV	max. μV/K	max. Ω	max. μV/V	min. dB	
BFQ10	TO-71	30	–	10	0,5 10	0,5 3,5	5	5	6	18	95	87
BFQ11							10	5	6	30	90	87
BFQ12							10	10	12	30	85	87
BFQ13							10	20	12	30	85	87
BFQ14							15	20	12	30	80	87
BFQ15							20	40	20	30	80	87
BFQ16							50	50	30	100	80	87
BFS21	SOT-52	30	10	0,5	1 –	– 6	20	75	15	1000	60	107
BFS21A							10	40	7,5	500	66	107

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS							page
		V_{DS}	I_G	I_{DSS}		$-V_{(P)GS}$		$R_{ds\,on}$	C_{rs}	t_{on}	t_{off}	
				min.	max.	min.	max.	max.	max.	max.	max.	
		V	mA	mA		V		Ω	pF	ns	ns	
BSJ111				20	–	3	10	30	–	–	–	145
BSJ112	TO-92	40	50	5	–	1	5	50	–	–	–	145
BSJ113				2	–	0,5	3	100	–	–	–	145
BSR56				50	–	4	10	25	–	9	25	153
BSR57	SOT-23	40	50	20	100	2	6	40	5	10	50	153
BSR58				8	80	0,8	4	60	–	20	100	153
BSR111				20	–	3	10	30	–	–	–	157
BSR112	SOT-23	40	50	5	–	1	5	50	–	–	–	157
BSR113				2	–	0,5	3	100	–	–	–	157
BSV78				50	–	3,75	11	25	–	10	10	165
BSV79	TO-18	40	50	20	–	2	7,0	40	5	18	16	165
BSV80				10	–	1	5,0	60	–	30	32	165
PMBF4391		40		50	150	4	10	30	–	15	20	173
PMBF4392	SOT-23	40	50	25	75	2	5	60	3,5	15	35	173
PMBF4393		40		5	30	0,5	3	100	–	15	50	173
PN4391				50	150	4	10	30	5	15	20	181
PN4392	TO-92	40	50	25	100	2	5	60	5	15	35	181
PN4393				5	60	0,5	3	100	5	15	50	181

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS								page
		V_{DS}	I_G	I_{DSS} min.	I_{DSS} max.	$-V_{(P)GS}$ min.	$-V_{(P)GS}$ max.	$R_{ds\,on}$ max.	C_{rs} max.	t_{on} max.	t_{off} max.	
		V	mA	mA		V		Ω	pF	ns	ns	
2N3966	TO-72	30	10	2	–	4	6	220	1,5	120	100	189
2N4091				30	–	5	10	30		25	40	193
2N4092	TO-18	40	10	15	–	2	7,0	50	5	35	60	193
2N4093				8	–	1	5,0	80		60	80	193
2N4391				50	150	4	10	30		15	20	197
2N4392	TO-18	50	50	25	75	2	5,0	60	3,5	15	35	197
2N4393				5	30	0,5	3,0	100		15	50	197
2N4856		40		50	–	4	10	25		9	25	201
2N4857		40		20	100	2	6	40		10	50	201
2N4858	TO-18	40	50	8	80	0,8	4	60	8	20	100	201
2N4859		30		50	–	4	10	25		9	25	201
2N4860		30		20	100	2	6	40		10	50	201
2N4861		30		8	80	0,8	4	60		20	100	201

P-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS							page
		$\pm V_{DS}$ V	I_G mA	I_{DSS} min. mA	I_{DSS} max. mA	$-V_{(P)GS}$ min. V	$-V_{(P)GS}$ max. V	$R_{ds\ on}$ max. Ω	C_{rs} max. pF	t_{on} max. ns	t_{off} max. ns	
BSJ174	TO-92	30	50	20	135	5	10	85	4	7	15	149
BSJ175				7	70	3	6	125		15	30	149
BSJ176				2	35	1	4	250		35	35	149
BSJ177				1,5	20	0,8	2,25	300		45	40	149
BSR174	SOT-23	30	50	20	135	5	10	85	4	7	15	161
BSR175				7	70	3	6	125		15	30	161
BSR176				2	35	1	4	250		35	35	161
BSR177				1,5	20	0,8	2,25	300		45	45	161
PMBFJ174	SOT-23	30	50	20	135	5	10	85	–	–	–	177
PMBFJ175				7	70	3	6	125	–	–	–	177
PMBFJ176				2	35	1	4	250	–	–	–	177
PMBFJ177				1,5	20	0,8	2,25	300	–	–	–	177

N-channel MOS-FETs single gate for switching

type number	envelope	RATINGS		CHARACTERISTICS						page
		V_{DS}	I_D	I_{DSS} min.	$-V_{(P)GS}$**	mode	$R_{ds\,on}$ max.	C_{rs} typ.	t_{on}/t_{off} typ.	
		V	mA	mA	V		Ω	pF	ns	
BFR29	TO-72	30*	20	10 – 40	0,5 – 3,5	depl	–	0,4	–	207
BSD10	TO-72	10	50	– –	– 2	depl	30	0,6	1/5	215
BSD12		20								215
BSD20	SOT-143	10	50	– –	– 2	depl	30	0,6	1/5	219
BSD22		20								219
BSD212	TO-72	10	50	– –	0,1 – 2	enh	70	0,6	1/5	223
BSD213		10								223
BSD214		20								223
BSD215		20								223
BSS83	SOT-143	10	50	– –	0,1 – 2	enh	45	0,6	1/5	227
BSV81	TO-72	30*	25	– –	– –	depl	100	0,5	–	231

* V_{DB}/V_{SB}
** enh. types $V_{GS(th)}$

N-channel MOS-FETs, dual gate

type number	envelope	RATINGS		CHARACTERISTICS							remarks	page
		V_{DS}	I_D	I_{DSS} min.	I_{DSS} max.	$-V_{(P)G1-S}$ max.	$\|y_{fs}\|$ f = 1 kHz min.	C_{is} typ.	C_{os} typ.	F typ.		
		V	mA	mA		V	mS			dB		
BF960*	SOT-103	20	20	2	20	3,5	9,5	1,8	0,9	2,8	UHF	239
BF964S*	SOT-103	20	50	4	20	2,5	15	2,5	1,0	1,0	VHF	243
BF965*	SOT-103	20	30	2	20	2,5	15	2,5	1,0	1,0	VHF	249
BF966S*	SOT-103	20	30	4	20	2,5	15	2,3	0,8	1,8	UHF	253
BF980A	SOT-103	18	30	–	–	1,3	17	2,6	1,1	2,8	UHF	259
BF981*	SOT-103	20	20	4	25	2,5	10	2,1	1,1	1,0	VHF	265
BF982*	SOT-103	20	40	–	–	1,3	20	4,0	2,0	1,2	VHF	273
BF989*	SOT-143	20	20	2	20	2,7	9,5	1,8	0,9	2,8	UHF	277
BF990A*	SOT-143	18	30	–	–	1,3	17	2,6	1,2	2,8	UHF	281
BF990AR*	SOT-143R	18	30	–	–	1,3	18	–	1,2	2,0	UHF	285
BF991*	SOT-143	20	20	4	25	2,5	10	2,1	1,1	1,0	VHF	287
BF992*	SOT-143	20	40	–	–	1,3	20	4,0	2,0	1,2	VHF	291
BF992R*	SOT-143R	20	40	–	–	1,3	20	–	2,0	1,2	VHF	297
BF994S	SOT-143	20	50	4	20	2,5	15	2,5	1,0	1,0	VHF	299
BF994SR*	SOT-143R	20	30	4	20	2,5	15	–	1,0	1,0	VHF	303
BF996S*	SOT-143	20	30	4	20	2,5	15	2,3	0,8	1,8	UHF	305
BF996SR*	SOT-143R	20	30	4	20	2,5	15	–	0,8	1,8	UHF	309
BF997*	SOT-143	20	30	2	20	2,5	15	2,5	1,0	1,0	VHF	311
BFR84*	TO-72	20	50	20	55	3,8	12	5,5	3,5	2,3	General purpose	315

* Protected against excessive input voltage surges.

N-channel vertical D-MOS-FETs for switching

type number	envelope	RATINGS				CHARACTERISTICS						page
		V_{DS}	I_D	P_{tot} at	T_{amb}	$V_{GS(th)}$	R_{DSon} @				t_{on}/t_{off}	
							typ.	max.	I_D	V_{GS}	max.	
		V	mA	mW	°C	V	Ω	Ω	mA	V	ns	
BS107	TO-92 var.	200	120	500	25	1,8 (typ.)	15	28	20	2,6	10/10	323
BS107A	TO-92 var.	200	250	600	25	1,0-3,0	4,5	6,4	250	10	5/15	327
BS170	TO-92 var.	60	500	830	25	0,8-3,0	2,5	5	200	10	10/10	331
BSN205	TO-92 var.	200	300	1000	25	0,8-2,8	3,5	6	300	20	10/20	339
BSN205A	TO-92 var.	200	300	1000	25	0,8-2,8	3,5	6	300	20	10/20	339
BSN254	TO-92 var.	250	300	1000	25	0,8-2,2	4,5	6	300	20	–	343
BSN254A	TO-92 var.	250	300	1000	25	0,8-2,2	4,5	6	300	20	–	343
BSS87	SOT-89	200	280	1000	25	0,8-2,8	4,5	6	280	20	10/25	351
BSS89	TO-92 var.	200	300	1000	25	0,8-2,8	4,5	6	300	20	–	355
BSS91	TO-18	200	350	1500	25*	0,8-2,8	4,5	6	350	20	15/25	359
BST70A	TO-92 var.	80	500	1000	25	1,5-3,5	2	4	500	10	10/15	367
BST72A	TO-92 var.	80	300	830	25	1,5-3,5	7	10	150	5	10/10	371
BST74A	TO-92 var.	200	300	1000	25	0,8-2,8	6	12	250	10	10/25	375
BST76A	TO-92 var.	180	300	1000	25	0,7-2,7	7	10	15	3	10/15	379
BST78	TO-126	450	750	15000	75**	2,0-4,0	10	14	100	10	10/100	383

* T_{case}.
** T_{mb}.

N-channel vertical D-MOS-FETs for switching

type number	envelope	RATINGS				CHARACTERISTICS						page
		V_{DS}	I_D	P_{tot} at	T_{amb}	$V_{GS(th)}$	R_{DSon} typ.	R_{DSon} max.	@ I_D	@ V_{GS}	t_{on}/t_{off} typ.	
		V	mA	mW	°C	V	Ω	Ω	mA	V	ns	
BST80	SOT-89	80	500	1000	25	1,5-3,5	2	4	500	10	10/15	387
BST82	SOT-23	80	175	300	25	1,5-3,5	7	10	150	5	10/10	391
BST84	SOT-89	200	250	1000	25	0,8-2,8	6	12	250	10	10/25	395
BST86	SOT-89	180	300	1000	25	0,7-2,7	7	10	15	3	10/15	399
BST95	TO-39	200	2000	10000	25*	1-3	1,8	2	1500	10	10/25*	403
BST97	TO-18	180	300	1500	25*	0,7-2,7	7	10	15	3	10/15	407
PH6659		35	750				1,5		300	5		427
PH6660	TO-92 var.	60	500	1000	25	0,8-2,0	1,8		300	5	10/10	427
PH6661		90	500				2,4		300	5		427
PMBF170	SOT-23	60	250	300	25	0,8-3,0	2,5	5	250	10	10/15	431
2N6659	TO-39	35	1400	6250	25*	0,8-2,0	1,5	5	300	5	10/20	435
2N6660	TO-39	60	1100	6250	25*	0,8-2,0	1,8	5	300	5	10/20	435
2N6661	TO-39	90	900	6250	25*	0,8-2,0	2,4	5,3	300	5	10/20	435

* T_{mb}.

P-channel vertical D-MOS-FETs for switching

type number	envelope	RATINGS				CHARACTERISTICS						page
		V_{DS}	I_D	P_{tot} at T_{amb}		$V_{GS(th)}$	R_{DSon} typ.	R_{DSon} max.	@ I_D	@ V_{GS}	t_{on}/t_{off} typ.	
		V	mA	mW	°C	V	Ω	Ω	mA	V	ns	
BS250	TO-92 var.	45	250	830	25	1-3,5	9	14	200	10	4/10	335
BST100	TO-92 var.	60	300	1000	25	1,5-3,5	4,5	6	200	10	4/20	411
BST110	TO-92 var.	50	300	830	25	1,5-3,5	7,5	10	200	10	4/20	415
BST120	SOT-89	60	300	1000	25	1,5-3,5	4,5	6	200	10	4/20	419
BST122	SOT-89	50	250	1000	25	1,5-3,5	7,5	10	200	10	4/20	423
BSS92	TO-92 var.	200	250	1000	25	0,8-2,8	10	20	250	20	–	363
BSP204	TO-92 var.	200	250	1000	25	0,8-2,8	10	15	250	20	–	347
BSP204A	TO-92 var.	200	250	1000	25	0,8-2,8	10	15	250	20	–	347

GENERAL

Type designation
Rating systems
s-parameters
TO-92 variant transistors on tape
Tape and reel specification for SOT-23, SOT-143 and SOT-89
Soldering recommendations for SOT-23, SOT-143 and SOT-89
Soldering recommendations for SOT-103
Thermal characteristics for SOT-23 and SOT-143

PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

"Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do."

A basic type number consists of:

TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
B. SILICON or other material with band gap of 1,0 to 1,3 eV.
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\ j\text{-}mb} > 15$ K/W)
D. TRANSISTOR; power, audio frequency ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\ j\text{-}mb} > 15$ K/W)
G. MULTIPLE OF DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\ j\text{-}mb} > 15$ K/W)
S. TRANSISTOR; low power, switching ($R_{th\ j\text{-}mb} > 15$ K/W)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
U. TRANSISTOR; power, switching ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
X. DIODE: multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter **W**)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.*
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.*
This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*
   The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage
   A. 1% (according to IEC 63: series E96)
   B. 2% (according to IEC 63: series E48)
   C. 5% (according to IEC 63: series E24)
   D. 10% (according to IEC 63: series E12)
   E. 20% (according to IEC 63: series E6)
   The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.
   The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*
   The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R. The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*
   The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER,* preceded by a hyphen (–)
   The NUMBER indicates the depletion layer in μm. The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER,* preceded by a stroke (/).
   The NUMBER indicates how many basic devices are assembled into the array.

* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

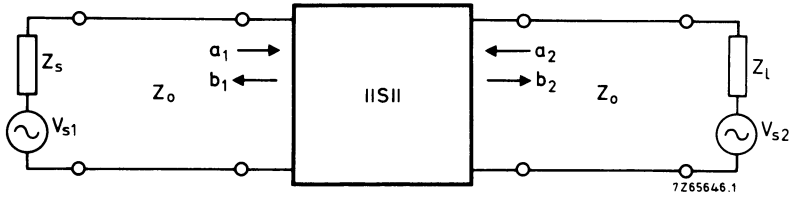
Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}} \qquad 1)$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \frac{b_1}{a_1}\bigg|_{a_2 = 0}$$
$$s_r = s_{12} = \frac{b_1}{a_2}\bigg|_{a_1 = 0}$$
$$s_f = s_{21} = \frac{b_2}{a_1}\bigg|_{a_2 = 0}$$
$$s_o = s_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o = 50\ \Omega$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o = 50\ \Omega$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o = 50\ \Omega$ and $V_{s2} = 0$.

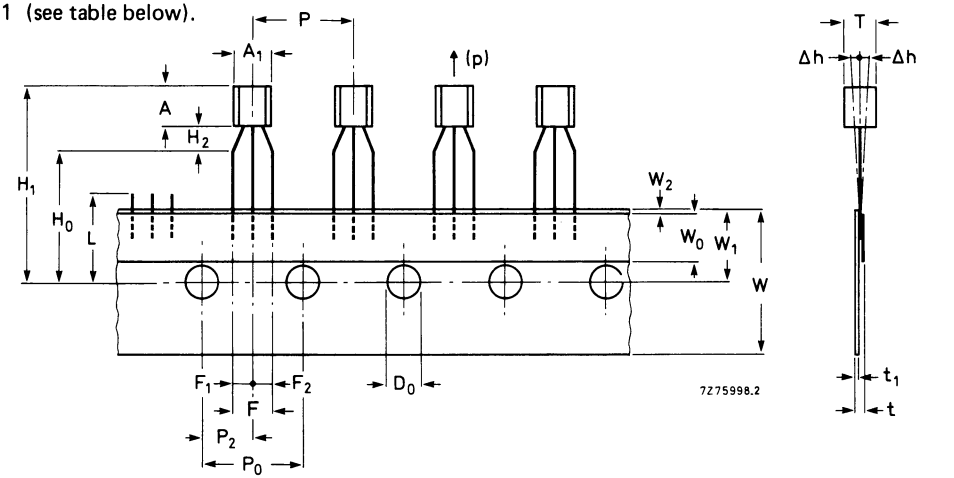
$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o = 50\ \Omega$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Dimensions in mm

Fig. 1 (see table below).



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A_1	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P_o		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P_2		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 −0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W_o		6		± 0,2	
Hole position	W_1		9		+ 0,7 −0,5	
Hold-down tape position	W_2		0,5		± 0,2	
Lead wire clinch height	H_o		16		± 0,5	
Component height	H_1			32,25		
Length of snipped leads	L			11,0		
Feed hole diameter	D_o		4		± 0,2	
Total tape thickness	t			1,2		t_1 0,3-0,6
Lead-to-lead distance	F_1, F_2		2,54		+ 0,4 −0,1	
Clinch height	H_2			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

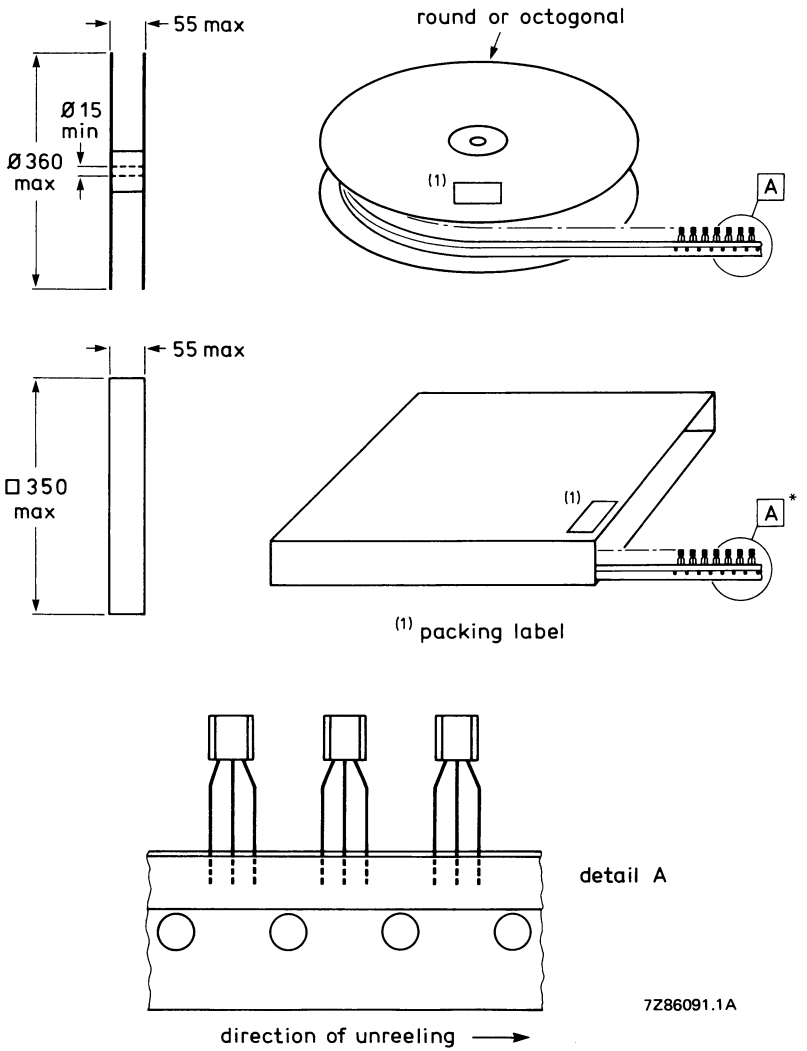


Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_o) is maintained (see Fig. 3).

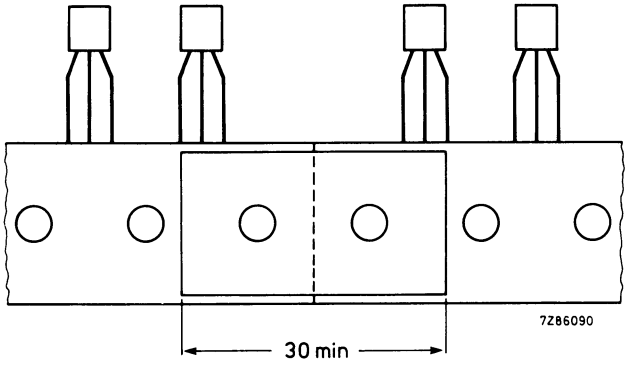


Fig. 3 Jointing tape with splicing patch.

* The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.

The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

TAPE AND REEL SPECIFICATION

Semiconductors in SOT-23, SOT-143 and SOT-89 encapsulations can be delivered in reel packing for aotomatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.

A separate reel packing for SOT-89 encapsulation is given in Fig. 3.

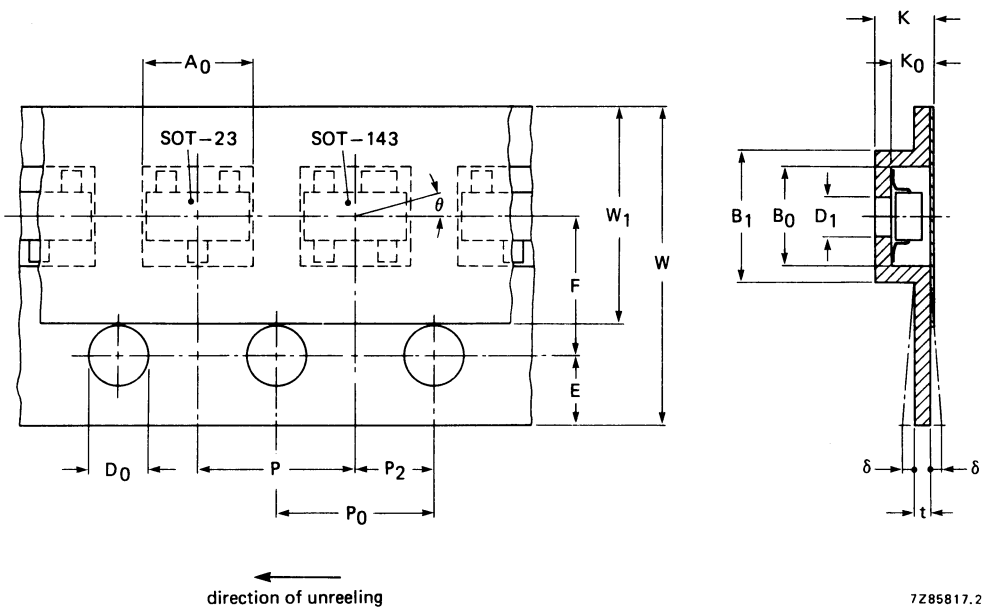


Fig. 1 Configuration of bandolier. Dimensions in mm.

Compartment			tol.
length	A_0	component length	+0,2
width	B_0	component width	+0,2
depth	K_0	0,95	+0,2
width outside	B_1	3,3	max.
pitch	P	4,0	±0,1
deviation	Θ	15°	max.
hole diameter	D_1	1	min.
Sprocket hole			
diameter	D_0	1,5	+0,1
pitch	P_0	4,0	±0,1
distance	E	1,75	±0,1
cumulative (10) pitch error		±0,1	

Centre line dimensions			tol.
length direction	P_2	2,0	±0,05
width direction	F	3,5	±0,05
Fixing tape			
width	W_1	5,5	±0,25
thickness	—	0,1	max.
Carrier tape			
width	W	8,0	±0,2
bending	δ	0,3	max.
thickness	t	0,4	max.
Overall thickness	K	1,5	max.

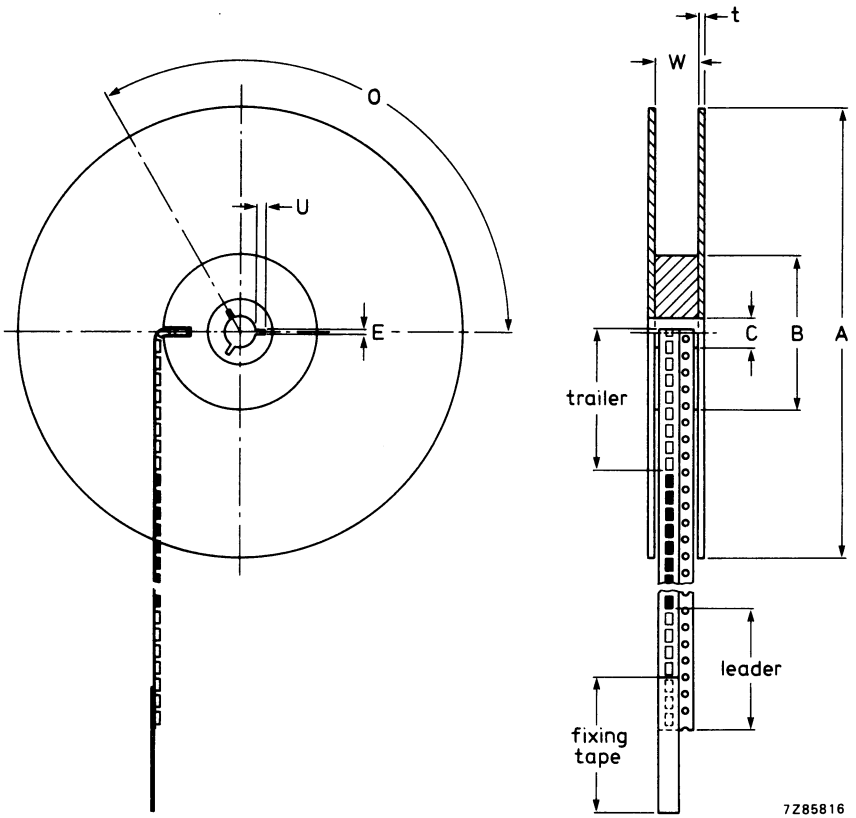


Fig. 2 Configuration of reel and flange (dimensions in mm).

Flange			tol.
diameter	A	180	+0 −2
thickness	t	1,5	+0,5 −0,1
space between flanges	W	9,5	± 0,5

Hub			tol.
diameter	B	62	± 1,5
spindle hole	C	12,75	+0,15 −0
key slit			
width	E	2	± 0,5
depth	U	4	± 0,5
location	O	120	degrees

Amount of devices per reel

The bandolier of a 180 mm reel contains at least 3000 devices with no more than 15 empty compartments (0,5%). Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.

The carrier tape (leader) starts with at least 75 empty positions (equivalent to 300 mm); the covering foil is at least 300 mm. In order to fix the carrier tape a self-adhesive tape of 20 to 50 mm is applied.

At the end of the bandolier (trailer) at least 75 empty positions (equivalent to a length of 300 mm) and 300 mm foil. For fixing onto the reel a self-adhesive tape of 20 to 50 mm is applied.

Semiconductors in SOT-89 encapsulations can also be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.Total number of devices per reel is 1000.

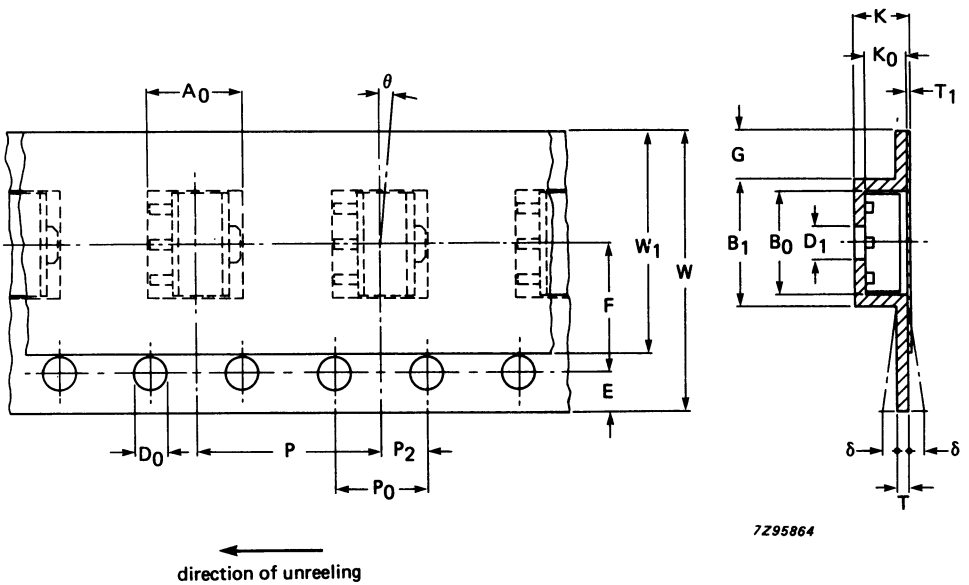


Fig. 3 Configuration of bandolier. Dimensions in mm.

Compartment			tol.
length	A_0	component length	
width	B_0	component width	
depth	K_0	component depth	
width outside	B_1	5,7	max.
pitch	P	8,0	± 0,1
deviation	Θ	± 5°	max.
hole diam.	D_1	1,5	min.
Sprocket hole			
diameter	D_0	1,5	+ 0,1
pitch	P_0	4,0	± 0,1
distance	E	1,75	± 0,1
cumulative (10) pitch error		± 0,1	

Centre line dimensions			tol.
length direction	P_2	2,0	± 0,05
width direction	F	5,5	± 0,1
Fixing tape			
width	W_1	9,5	max.
thickness	T_1	0,1	max.
Carrier tape			
width	W	12	± 0,2
bending	δ	0,3	max.
thickness	T	0,4	max.
Overall thickness	K	2,4	max.
distance	G	1,8	min.

SOLDERING RECOMMENDATIONS
SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.
The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C.
The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrally arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

WAVE SOLDERING

The normal (dual) wave soldering process can also be aplied to SOT-23 and SOT-143 envelopes
We do not recommend SOT-89 for wave soldering.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

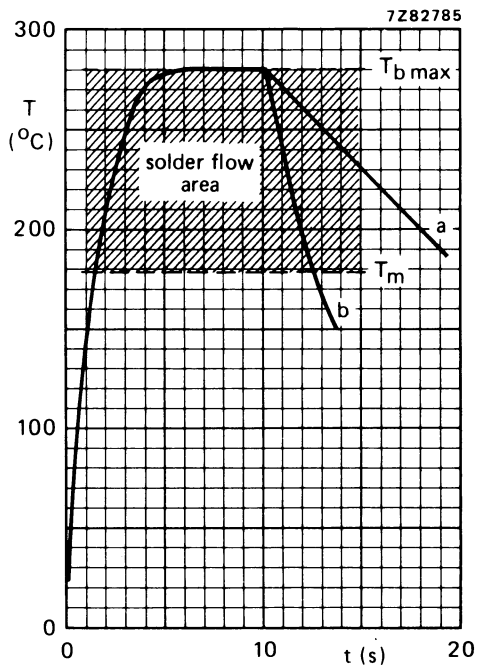
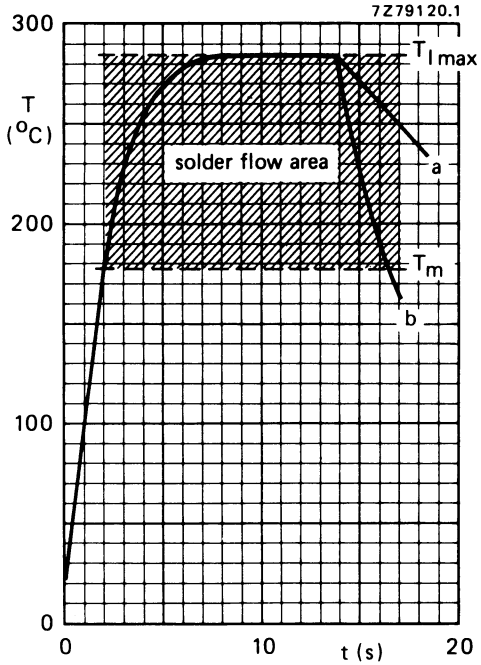


Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.
a = free convection cooling; b = forced cooling.
$T_{b\ max}$ = maximum bath temperature (280 °C).
T_m = melting temperature of solder (179 °C).



a = free convection cooling.

b = permissible forced cooling.

$T_{l\,max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:
without preheating max. 14 s
with preheating max. 10 s

Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

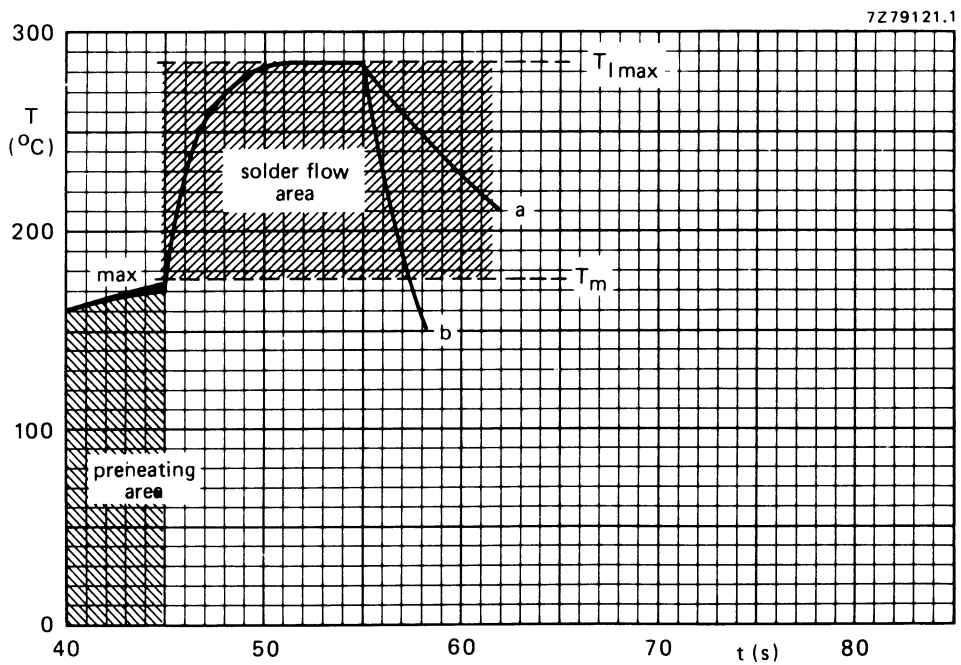


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

Dimensions in mm

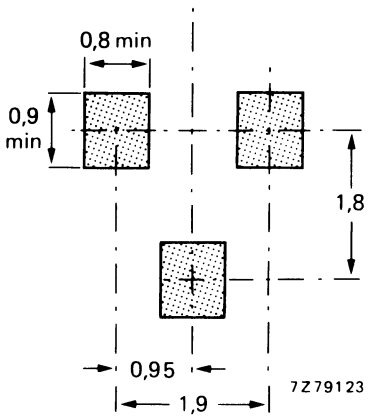


Fig. 4 SOT-23 pattern.

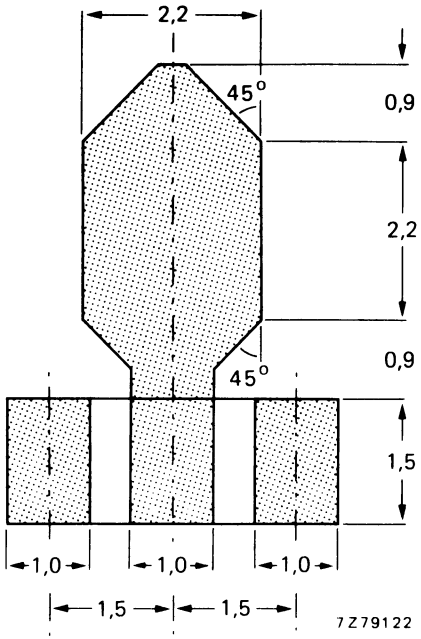


Fig. 5 SOT-89 pattern.

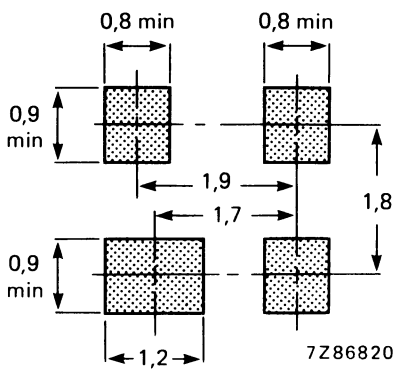


Fig. 6 SOT-143 pattern.

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

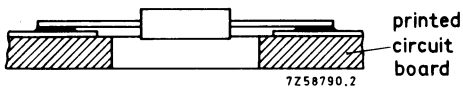


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

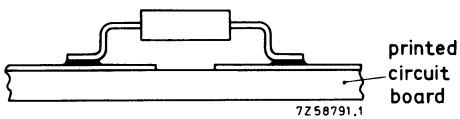


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

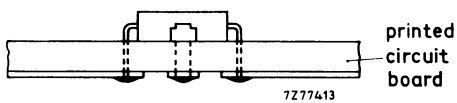


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s

THERMAL CHARACTERISTICS OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

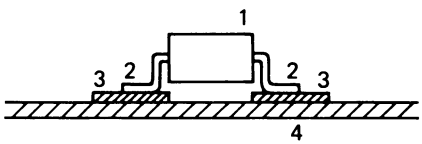


Fig. 1.

1. Heat radiation from the envelope to ambient (1).
   This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).

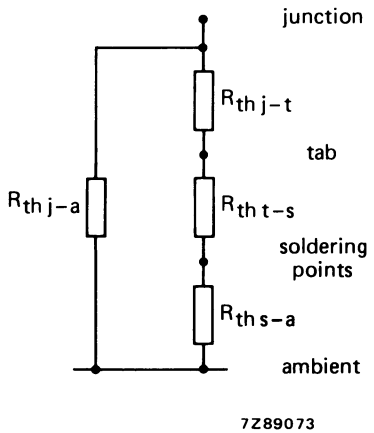


Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

$R_{th\ j\text{-}t}$ = Thermal resistance from junction to tab.

$R_{th\ t\text{-}s}$ = Thermal resistance from tab to soldering points.

$R_{th\ s\text{-}a}$ = Thermal resistance from soldering points to ambient.

$R_{th\ j\text{-}a}$ = Thermal resistance from junction to ambient.

Heat transfer directly from envelope to ambient

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.
Thus the thermal model can be as in Fig. 3.

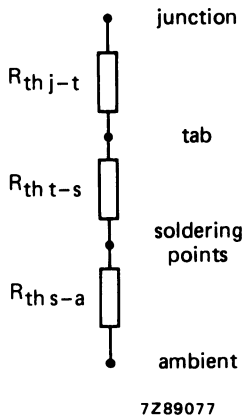


Fig. 3 Basic thermal model.

Heat transfer from junction to tab

This is an internal heat transfer and has been measured. In general it is:

for high-frequency transistors, low-power diodes and (MOS) FETs	60 K/W
for low-frequency and switching transistors	50 K/W
for low-frequency medium-power transistors	30 K/W

Heat transfer from tab to soldering points

This value has also been measured for SOT-23 with $P_{tot} < 350$ mW	280 K/W
for types of semiconductors in this envelope with $P_{tot} < 425$ mW	260 K/W
for types of semiconductors in a SOT-143 envelope this value is	310 K/W

Heat transfer from soldering points to ambient

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.

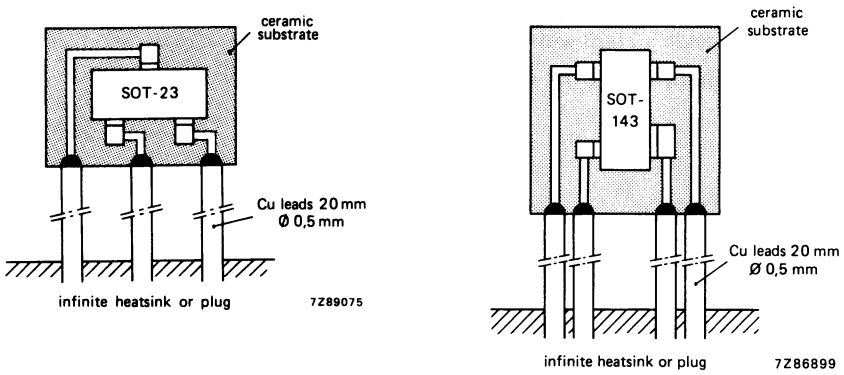


Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.

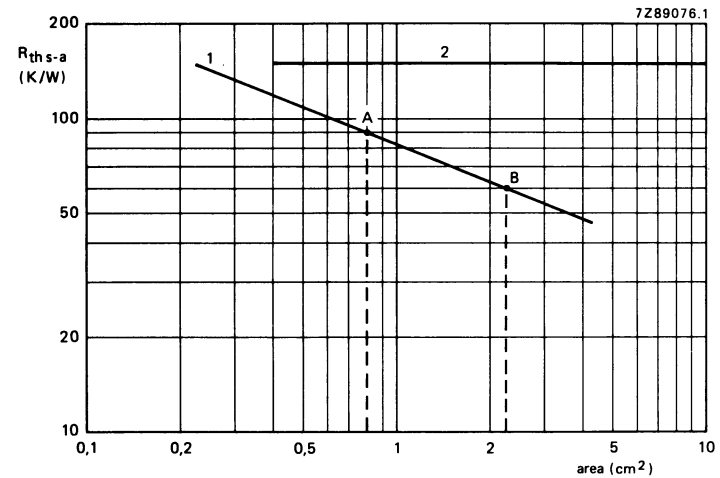


Fig. 5 Heat transfer from soldering points to ambient.

1. Ceramic substrate

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.
Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

2. Printed circuit board

$R_{th\ s\text{-}a}$ = 150 K/W for SOT-23 and SOT-143 envelopes mounted on a printed circuit board.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.
The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$$

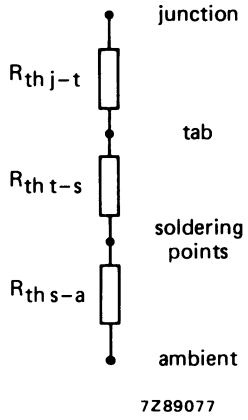


Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

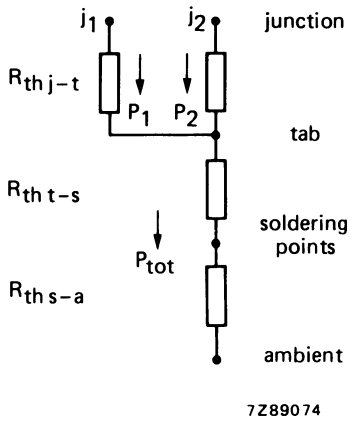


Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb} = P_{tot}\,(280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j\text{-}t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j\text{-}t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j\text{-}t}$ for diodes is 60 K/W.

$R_{th\ s\text{-}a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t\text{-}s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60\,P_1 + 370\,P_{tot} + T_{amb}$$

$$T_{j2} = 60\,P_2 + 370\,P_{tot} + T_{amb}$$

DEVICE DATA
J-FETs

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

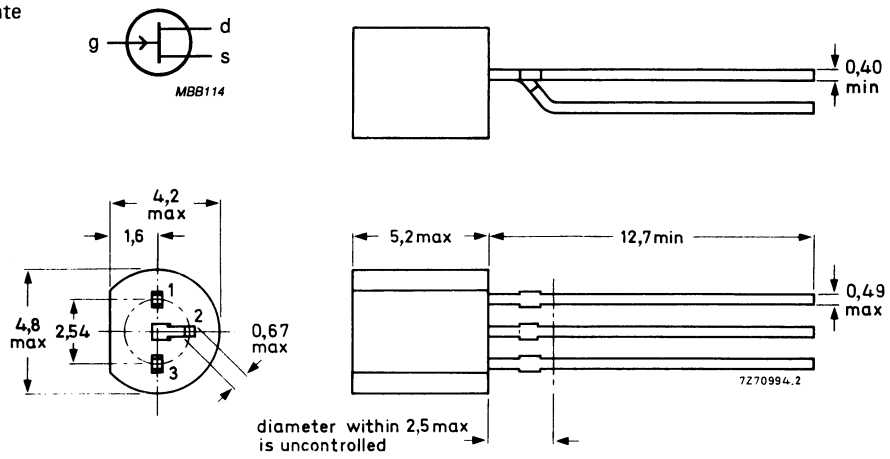
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 °C
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 12 mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	typ.	3,5 mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 1 kHz; R_G = 1 MΩ	F	<	2 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

→ From junction to ambient in free air	$R_{th\ j-a}$	=	**420**	**K/W**

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Drain current [1]							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 µA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\lvert y_{fs} \rvert$	>	2,5	3,0	3,5	4,0	mS
V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz							
Input capacitance	C_{is}		typ.	4.0			pF
Feedback capacitance	C_{rs}		typ.	1,2			pF
Output capacitance	C_{os}		typ.	1,6			pF
Noise figure at f = 1 kHz; R_G = 1 MΩ							
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C	F		typ.	0,5			dB
			<	2			dB
Equivalent noise voltage at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n/\sqrt{B}$		typ.	40			$nV/\sqrt{Hz}$

[1] Measured under pulse conditions.

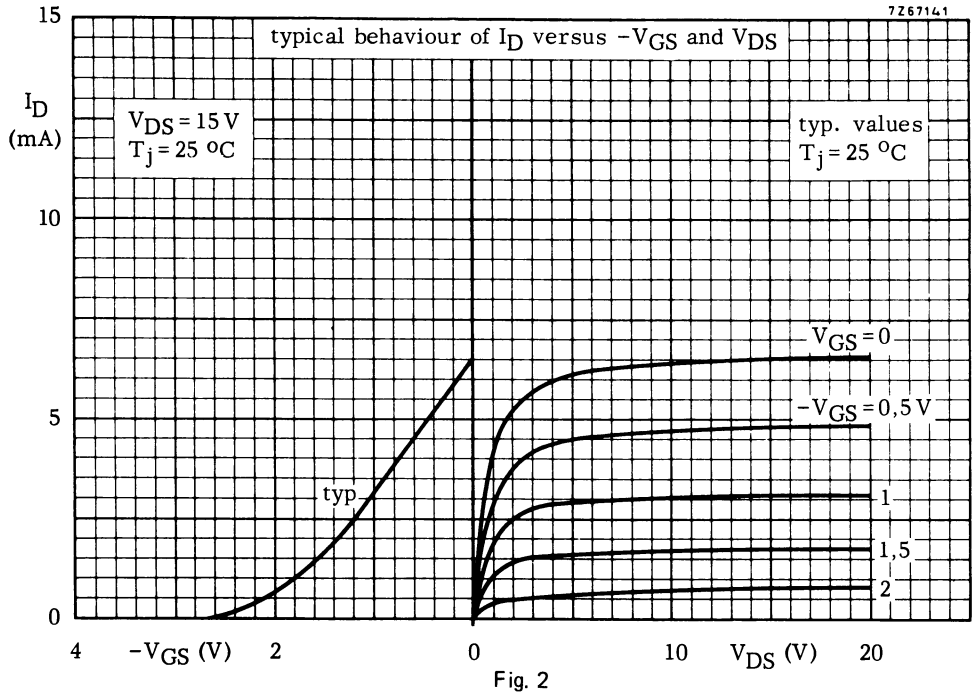


Fig. 2

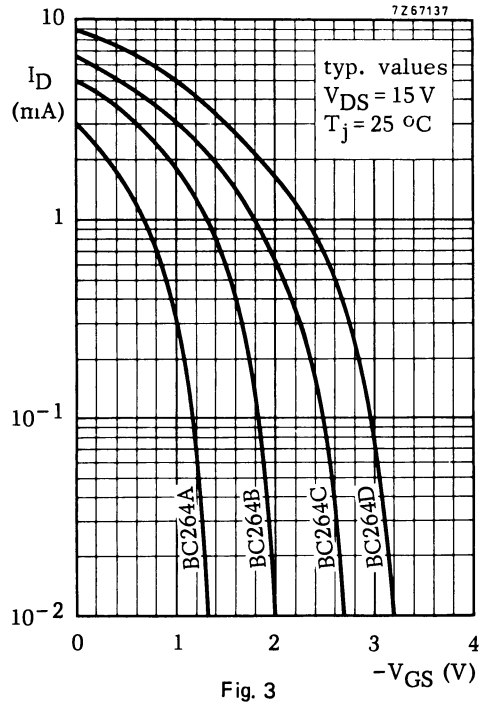


Fig. 3

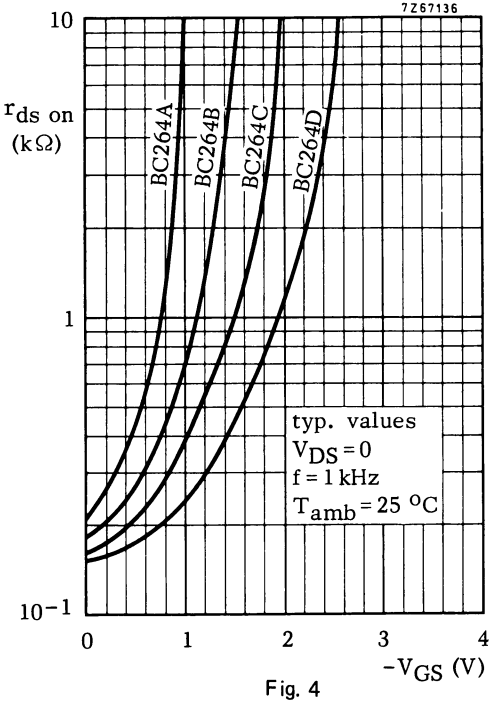


Fig. 4

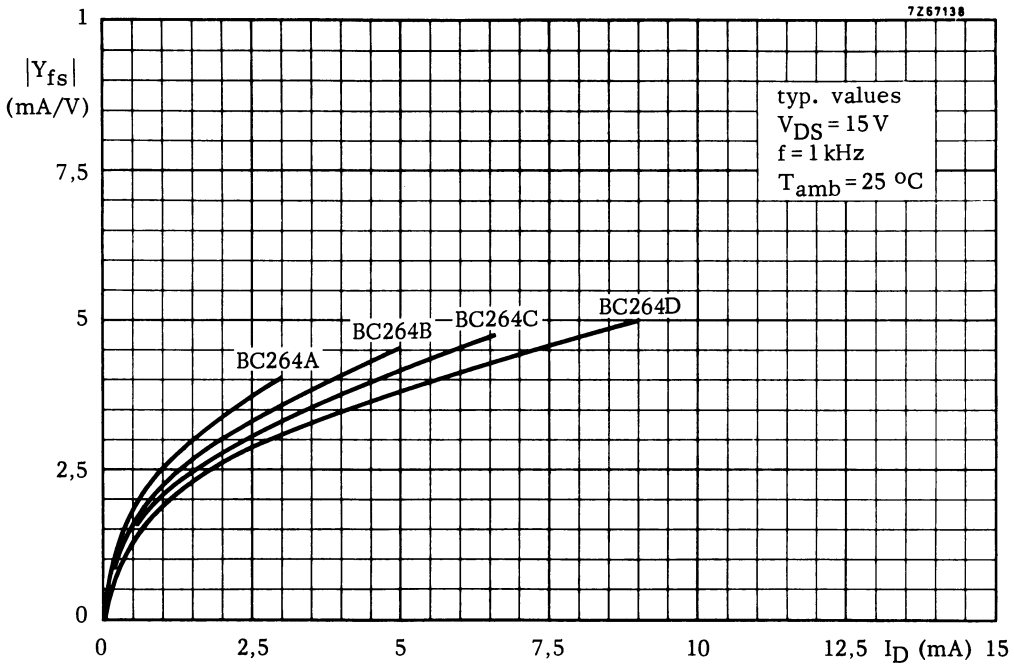


Fig. 5

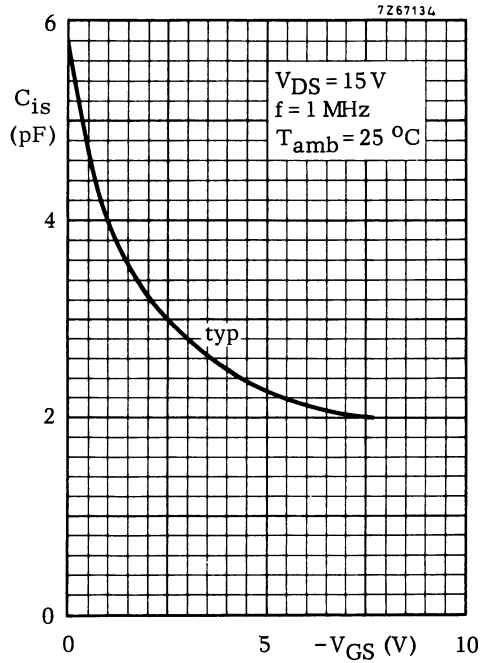


Fig. 6

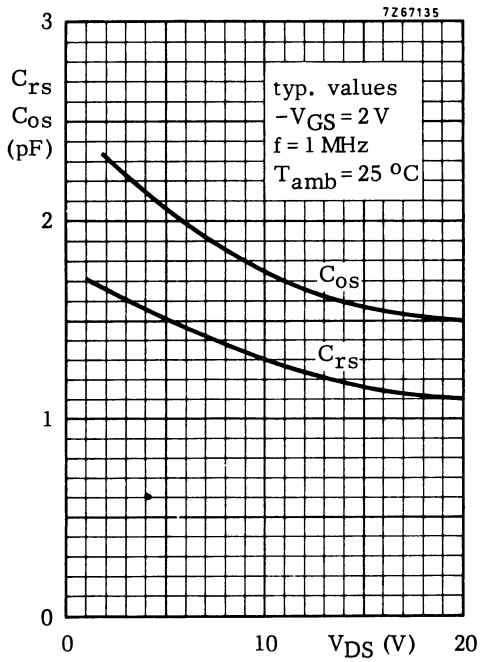


Fig. 7

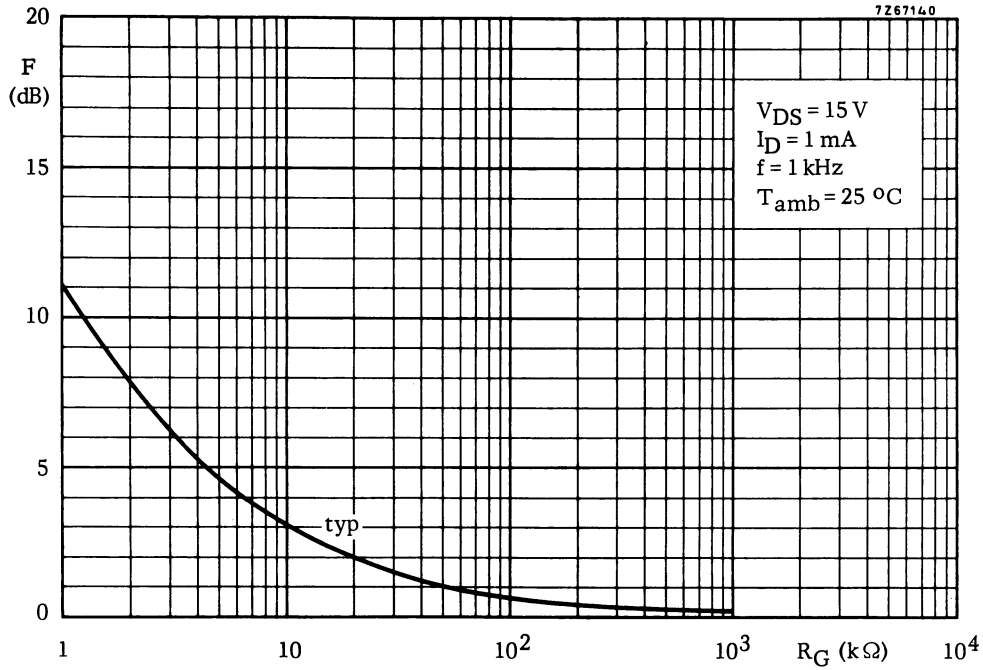

7Z67140
20
F
(dB)
15
10
5
0
1
10
10^2
10^3
10^4
R_G (kΩ)
typ
V_{DS} = 15 V
I_D = 1 mA
f = 1 kHz
T_{amb} = 25 °C

Fig. 8

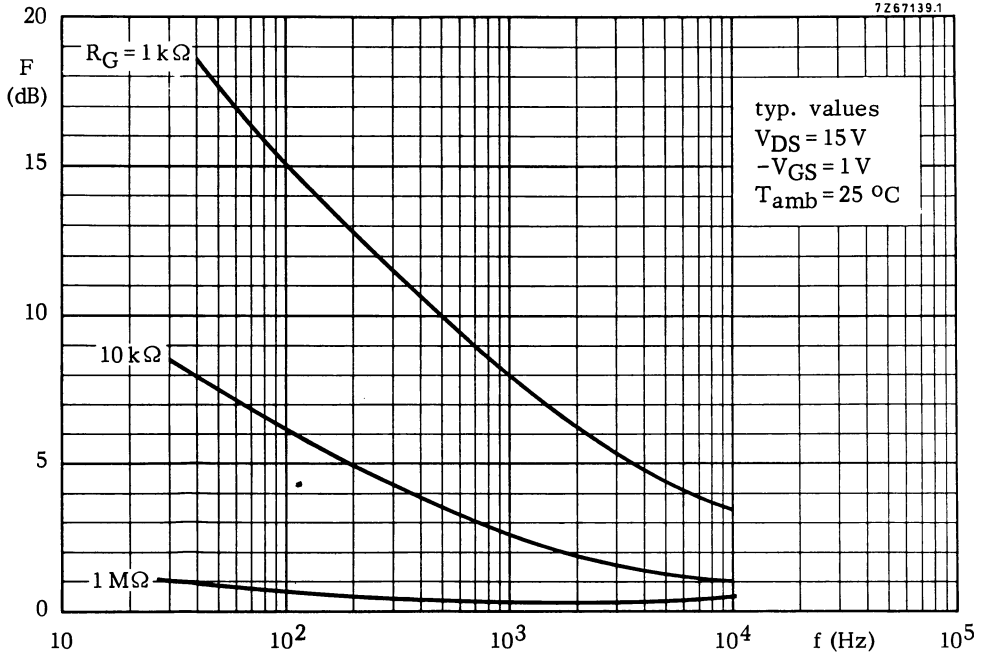

7Z67139.1
20
F
(dB)
15
10
5
0
10
10^2
10^3
10^4
10^5
f (Hz)
R_G = 1 kΩ
10 kΩ
1 MΩ
typ. values
V_{DS} = 15 V
$-V_{GS}$ = 1 V
T_{amb} = 25 °C

Fig. 9

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

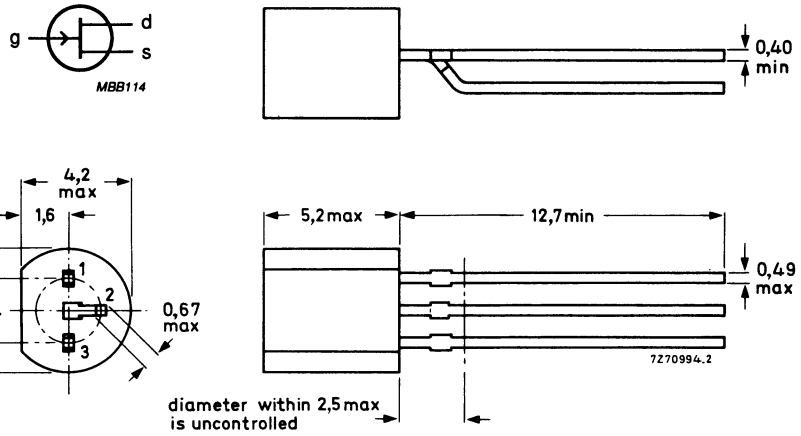
Drain-source voltage	$\pm V_{DS}$			max. 30		V
Gate-source voltage (open drain)	$-V_{GSO}$			max. 30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}			max. 300		mW
		BF245A/0	A	B	C	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 0,5	2,0	6	12	mA
		< 2,1	6,5	15	25	mA
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,25 to 8,0		V
Feedback capacitance at f = 1 MHz						
V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}			typ. 1,1		pF
Transfer admittance (common source)						
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$			3,0 to 6,5		mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	200 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C
Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5 nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5 μA
Drain current 2)				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	> 2	6,0	12 mA
		< 6,5	15,0	25 mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30 V
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)	> 0,4	1,6	3,2 V
		< 2,2	3,8	7,5 V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF245A/0: I_{DSS} = 0,5 to 2,1 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 1,9 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

Gate-source cut-off voltage				
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0	V
y-parameters at T_{amb} = 25 °C (common source)				
V_{DS} = 15 V; V_{GS} = 0				
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5	mS
	Output admittance	$\|y_{os}\|$	typ. 25	μS
f = 200 MHz	Input conductance	g_{is}	typ. 250	μS
	Reverse transfer admittance	$\|y_{rs}\|$	typ. 1,4	mS
	Transfer admittance	$\|y_{fs}\|$	typ. 6	mS
	Output conductance	g_{os}	typ. 40	μS
V_{DS} = 20 V; $-V_{GS}$ = 1 V				
f = 1 MHz	Input capacitance	C_{is}	typ. 4,0	pF
	Feedback capacitance	C_{rs}	typ. 1,1	pF
	Output capacitance	C_{os}	typ. 1,6	pF
Cut-off frequency *				
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ. 700	MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)				
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ. 1,5	dB

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

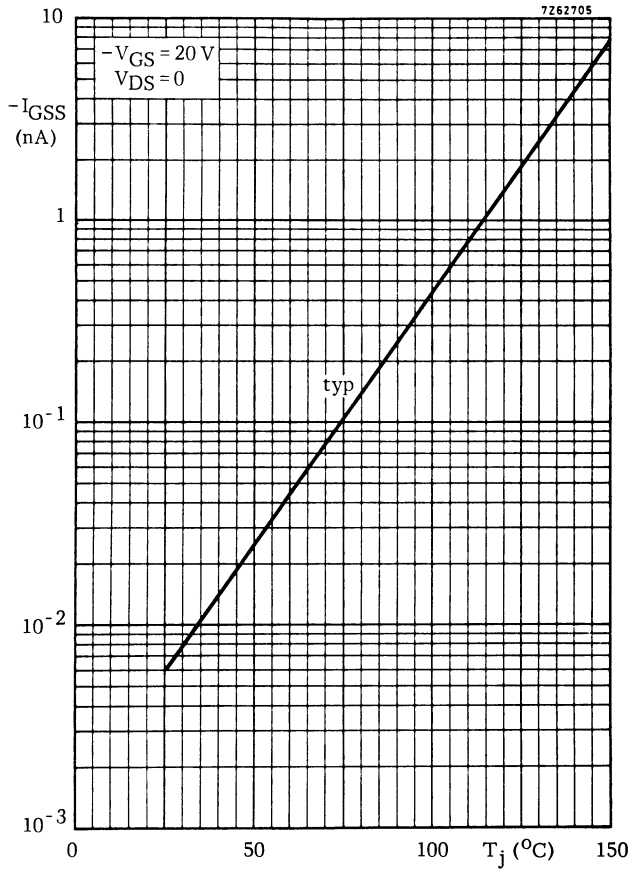

7Z62705
10
$-V_{GS}$ = 20 V
V_{DS} = 0
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

Fig. 2

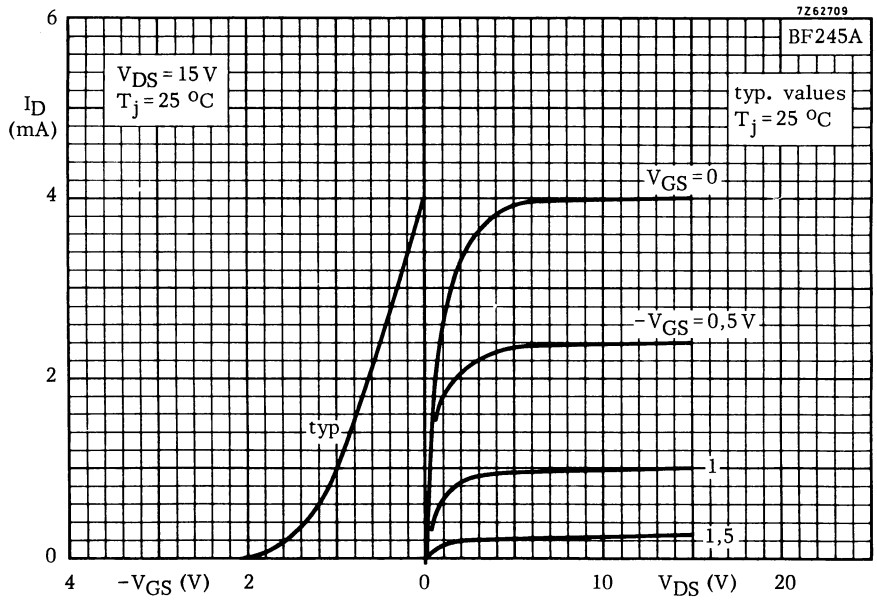

7Z62709
BF245A
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

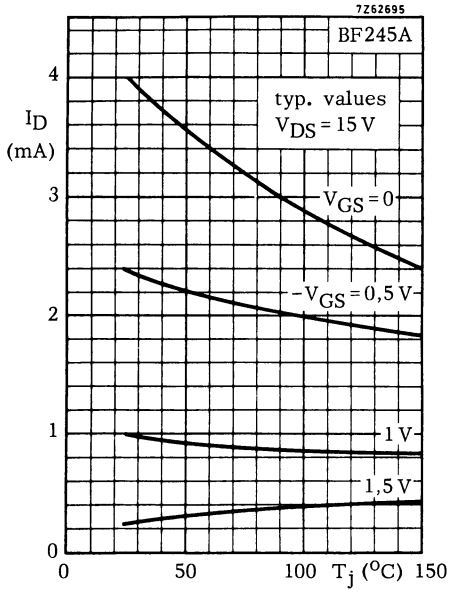

7Z62695
BF245A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
4
3
2
1
0
0
50
100
T_j (°C)
150

Fig. 4

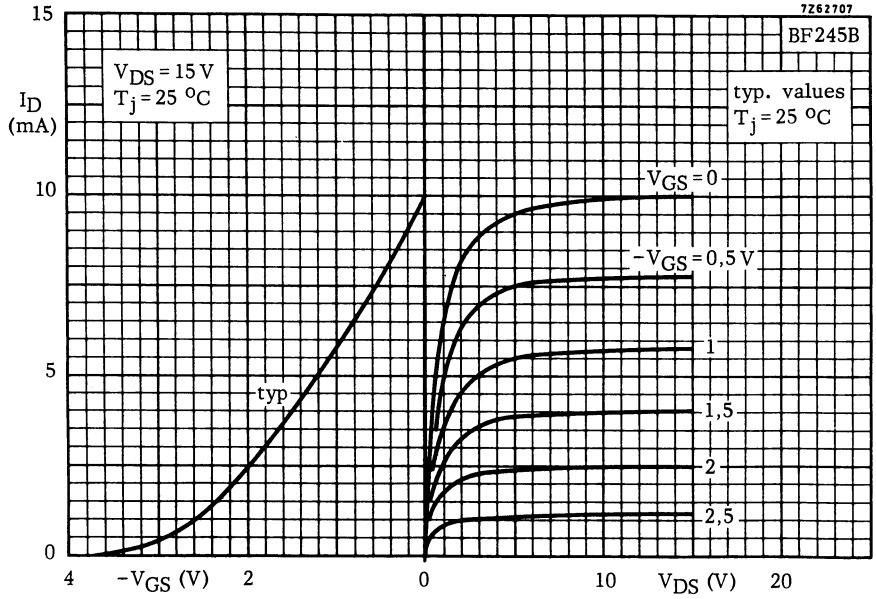

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
$-V_{GS}$ = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

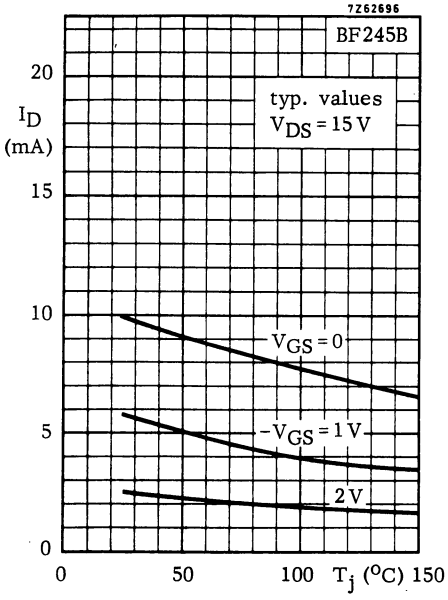

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

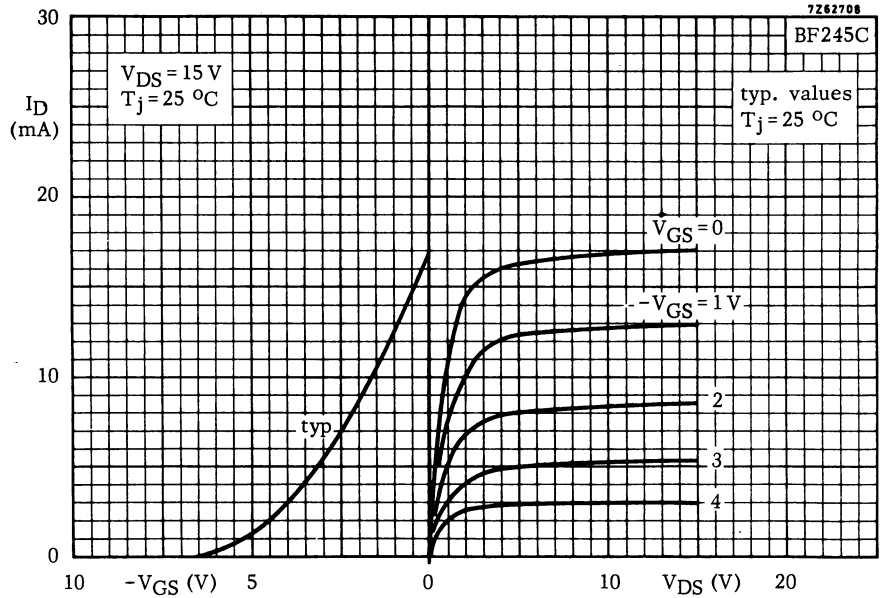

7Z62708
BF245C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
30
20
10
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

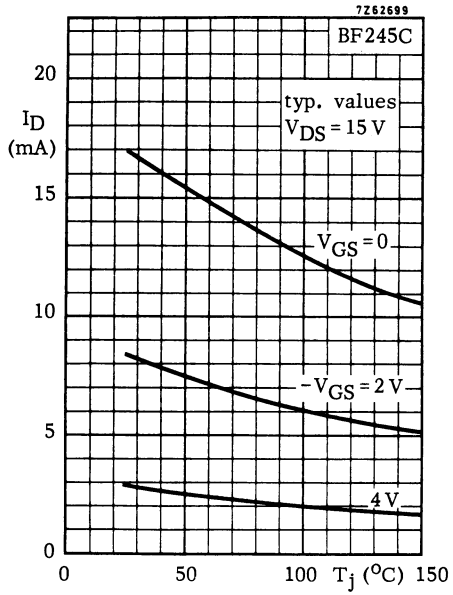

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

Fig. 8

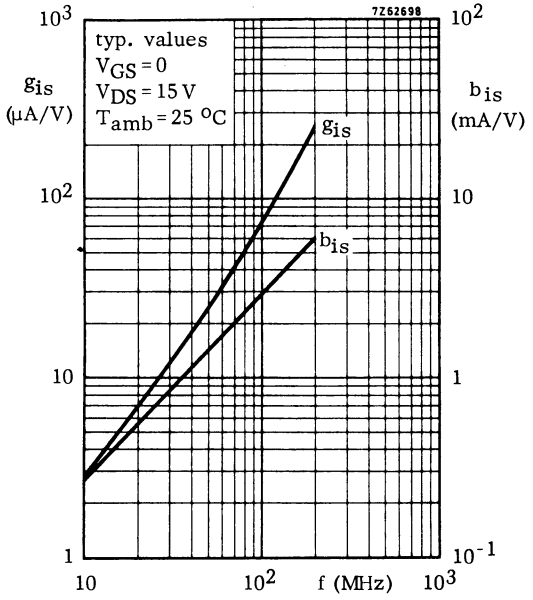

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

Fig. 9

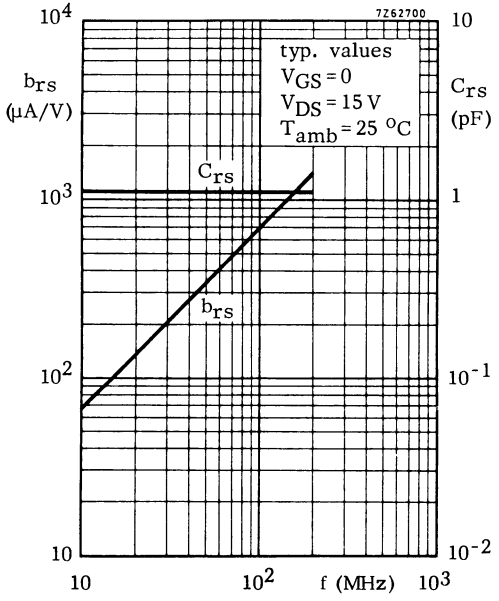

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 10

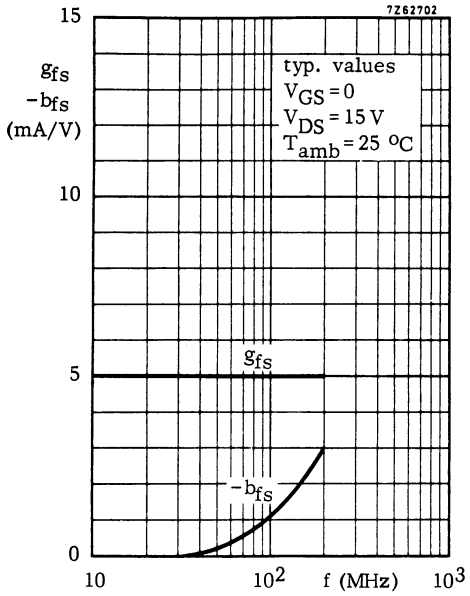

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

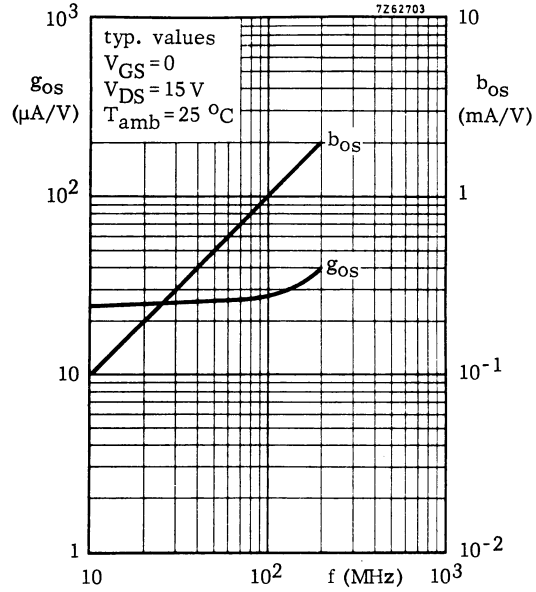

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
10
1
b_{os}
(mA/V)
10^{-1}
10^{-2}
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

Fig. 12

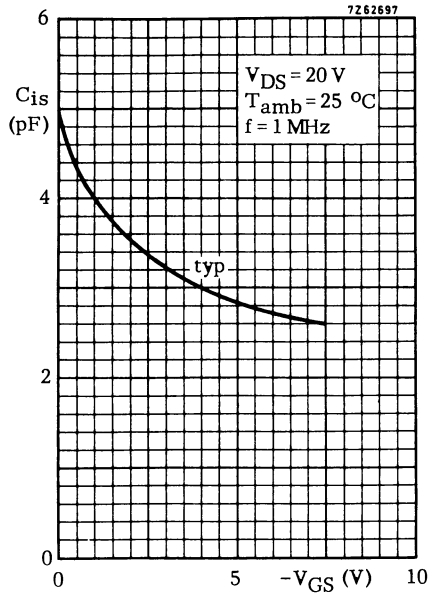


Fig. 13

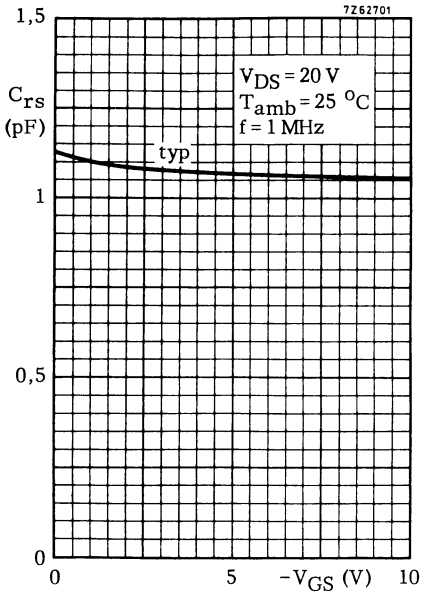


Fig. 14

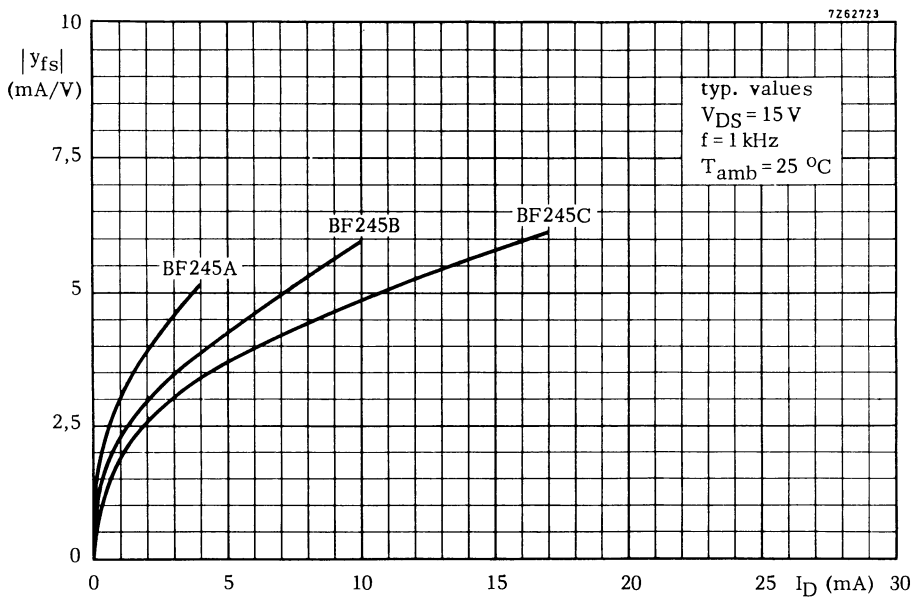


Fig. 15

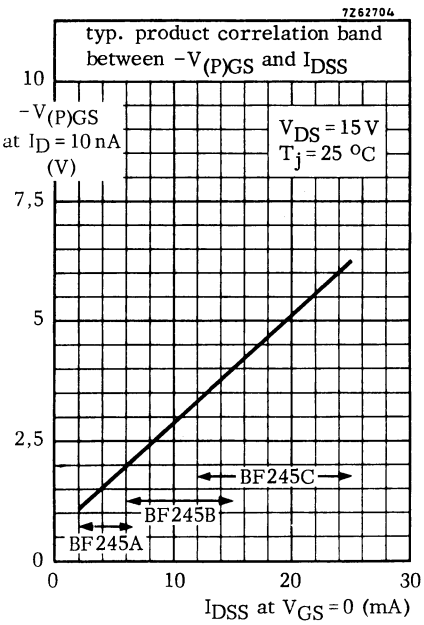


Fig. 16

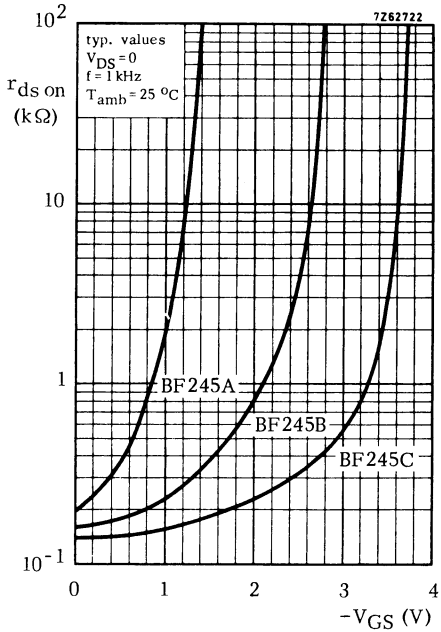


Fig. 17

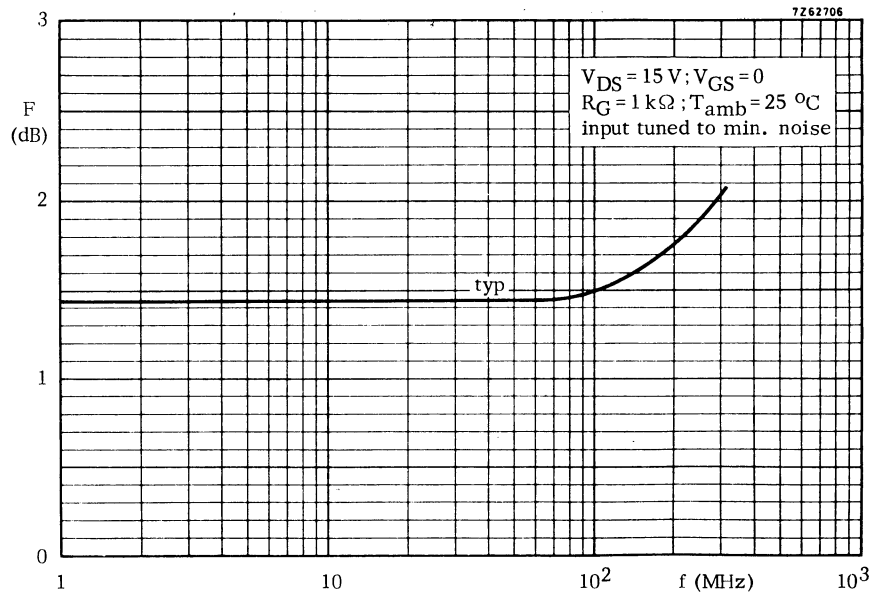


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

QUICK REFERENCE DATA

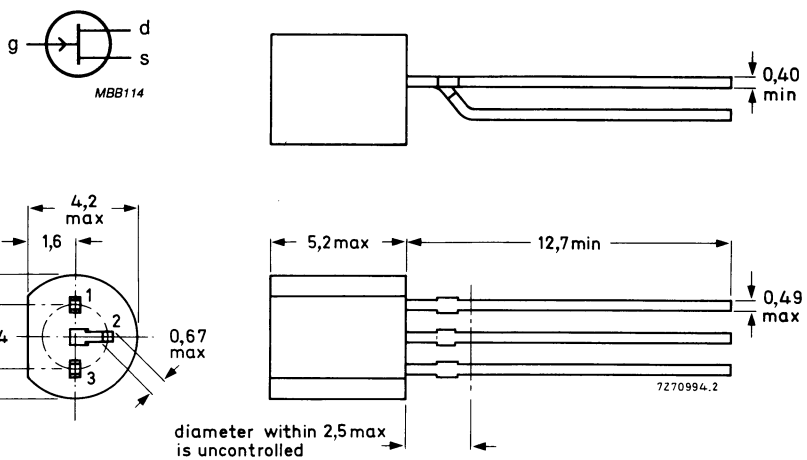
Drain-source voltage	$\pm V_{DS}$	max.		25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		250	mW
		BF247A	B	C	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 30	60	110	mA
		< 80	140	250	mA
Gate-source cut-off voltage					
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$		0,6 to 14,5		V
Feedback capacitance at f = 1 MHz					
I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.		3,5	pF
Transfer admittance (common source)					
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	>		8	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate current	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

CHARACTERISTICS

T_{amb} = 25 °C

			BF247A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	30	60	110	mA
		<	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	>	1,5	3,0	5,5	V
		<	4,0	7,0	12,0	V
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,6 to 14,5		V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>			8	mS
		typ.			17	mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V						
feed-back capacitance	C_{rs}	typ.			3,5	pF
input capacitance	C_{is}	typ.			11	pF
output capacitance	C_{os}	typ.			5	pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.			450	MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0{,}02$.

** The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

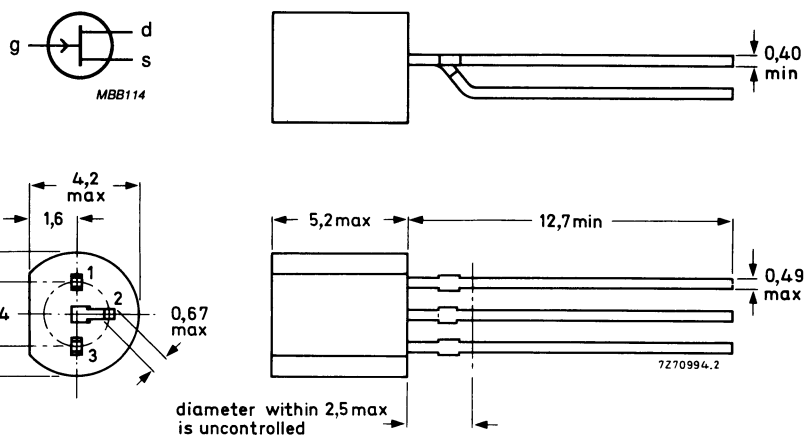
Drain-source voltage	$\pm V_{DS}$		max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$		max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}		max.	300	mW
		BF256A	B	C	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>3	6	11	mA
		<7	13	18	mA
Feedback capacitance at f = 1 MHz					
V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}		typ.	0,7	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|y_{fs}\|$		>	4,5	mS
Power gain at f = 800 MHz					
V_{DS} = 15 V; R_S = 47 Ω	G_p		typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W 1)

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<			5	nA
		BF256A		B	C	
Drain current 2)						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	>	3	6	11	mA
		<	7	13	18	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>			30	V
Gate-source voltage						
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)				0,5 to 7,5	V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF256B/1: I_{DSS} = 6 to 8 mA; $-V_{GS}$ = 1,4 to 2,6 V.

y-parameters (common source)			
Transistor admittance at f = 1 kHz			
V_{DS} = 15 V; V_{GS} = 0	$\|y_{fs}\|$	>	4,5 mS 1)
		typ.	5 mS 1)
Output capacitance at f = 1 MHz			
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF
Cut-off frequency			
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz 2)
Noise figure at f = 800 MHz			
V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB
Power gain at f = 800 MHz			
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB

1) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

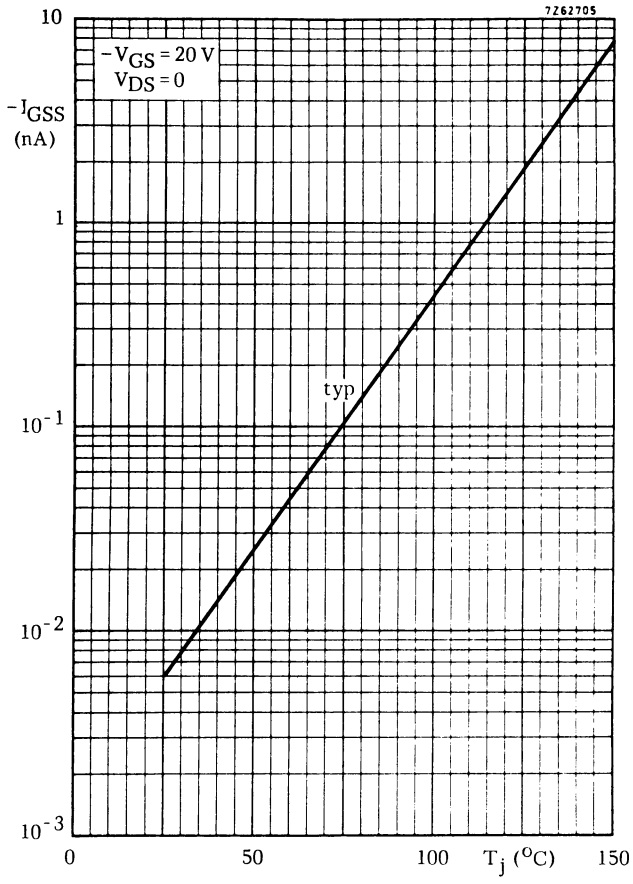

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (^{O}C)
150

Fig. 2

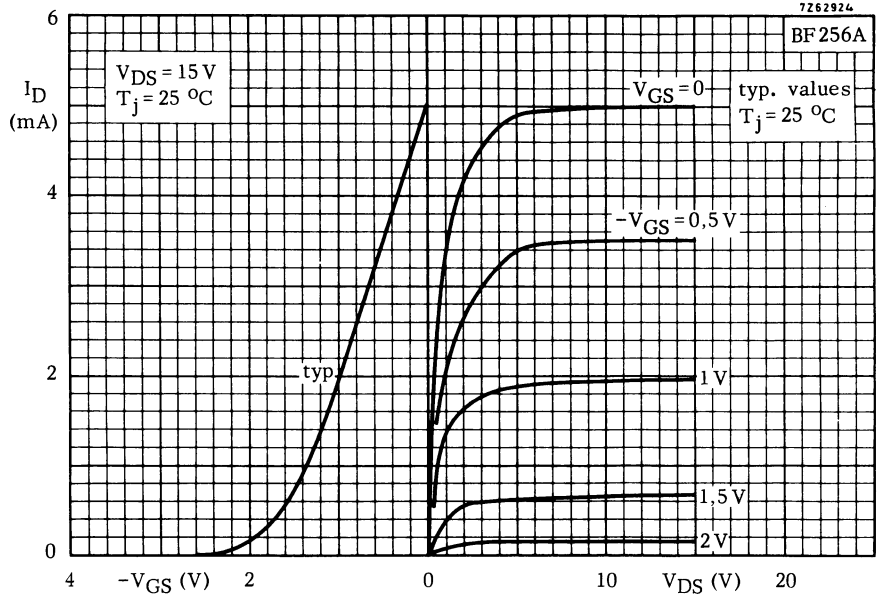

7Z62924
BF256A
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

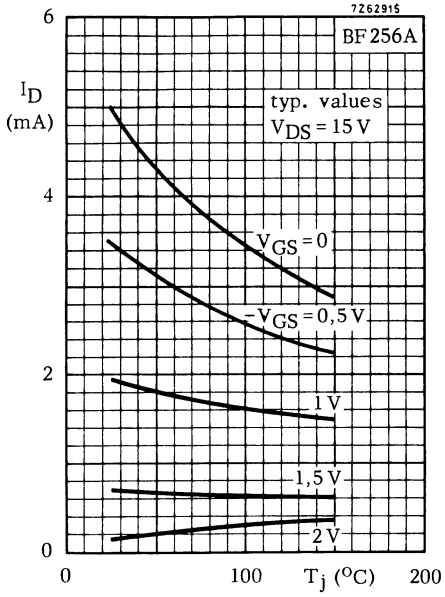

7Z62915
BF256A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
6
4
2
0
0
100
T_j (°C)
200

Fig. 4

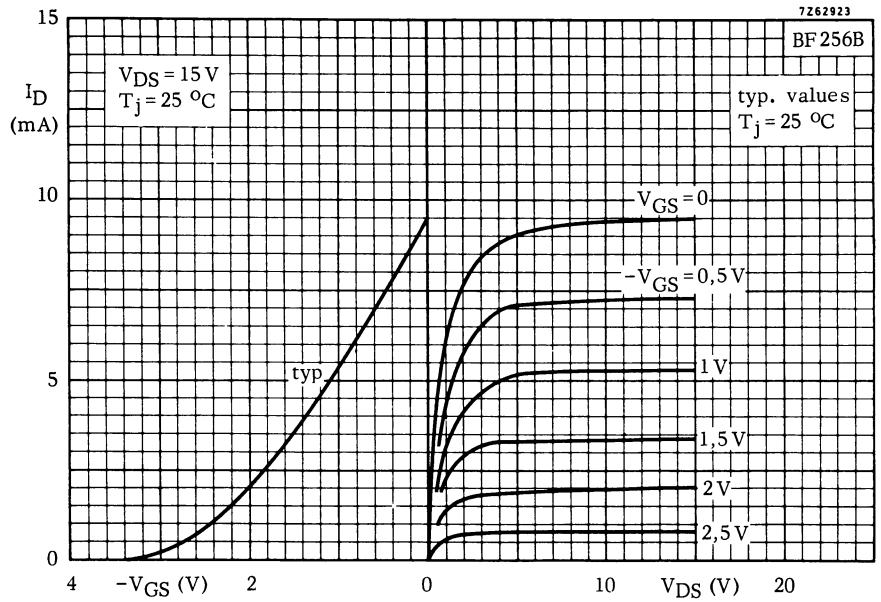

7Z62923
BF256B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
2,5 V
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

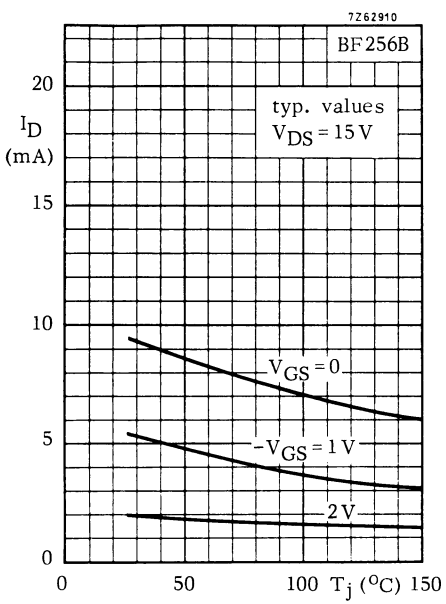

7Z62910
BF256B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

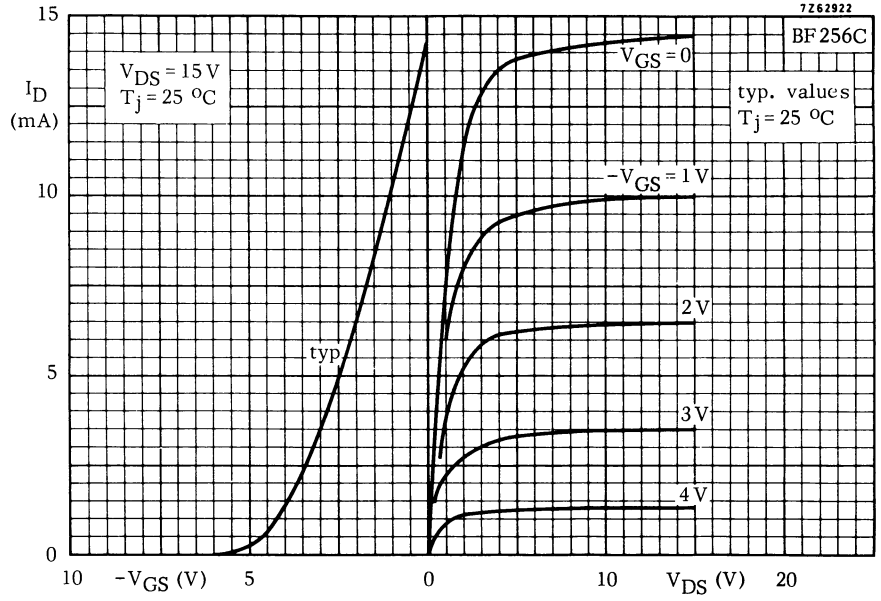

7Z62922
BF256C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
3 V
4 V
typ
15
10
5
0
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

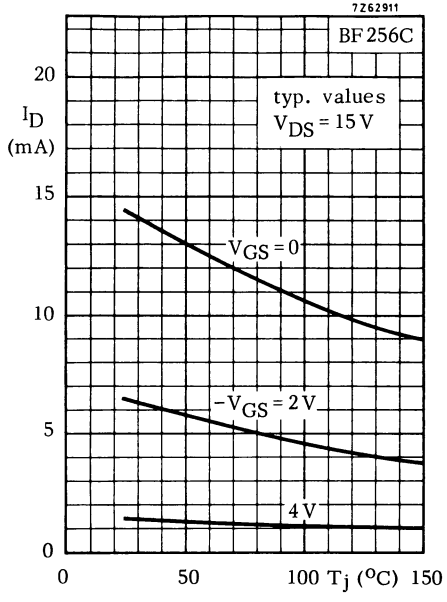

7Z62911
BF256C
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
20
15
10
5
0
0
50
100
T_j (°C)
150

Fig. 8

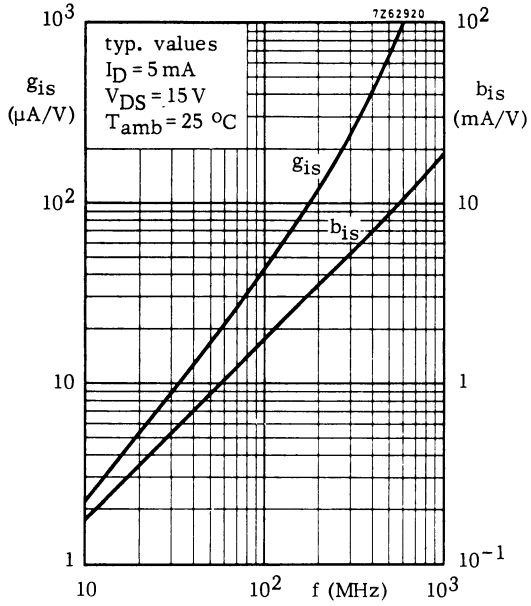

7Z62920
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

Fig. 9

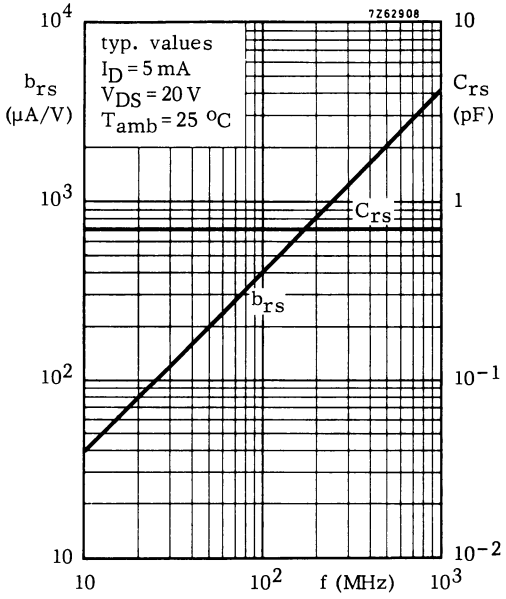

7Z62908
typ. values
I_D = 5 mA
V_{DS} = 20 V
T_{amb} = 25 °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 10

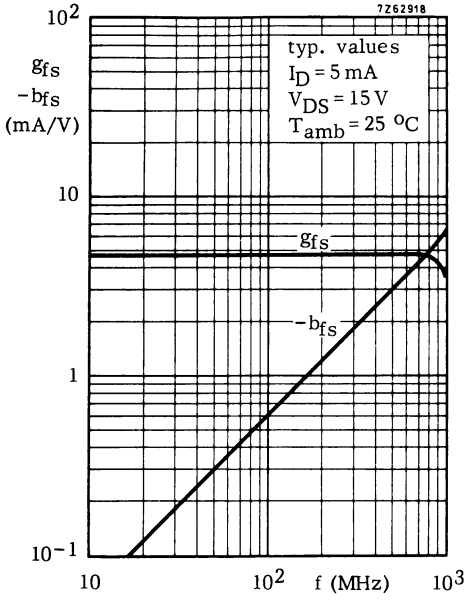

7Z62918
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{fs}
$-b_{fs}$
(mA/V)
10^2
10
1
10^{-1}
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

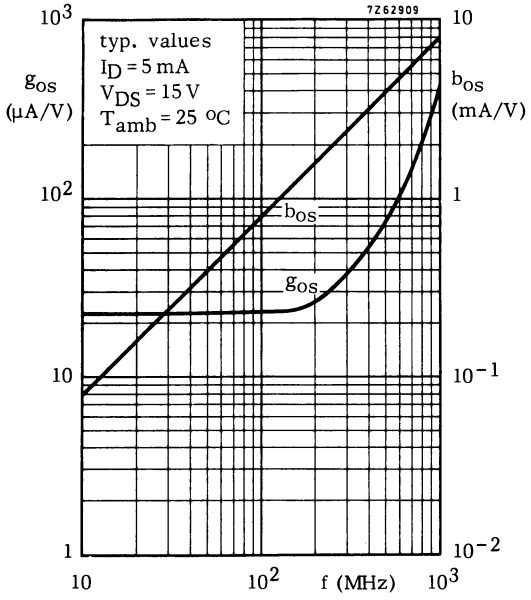

7Z62909
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{os}
(μA/V)
b_{os}
(mA/V)
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

Fig. 12

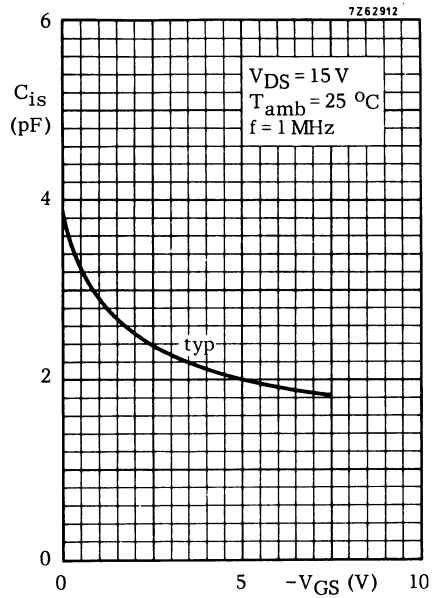


Fig. 13

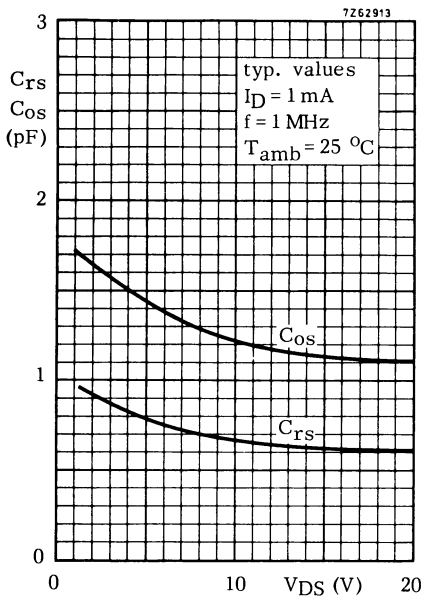


Fig. 14

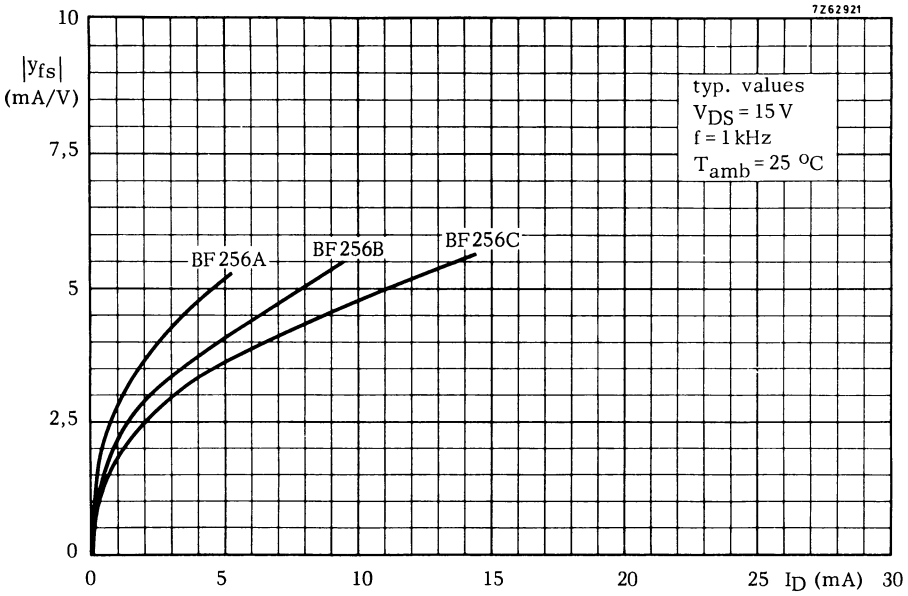


Fig. 15

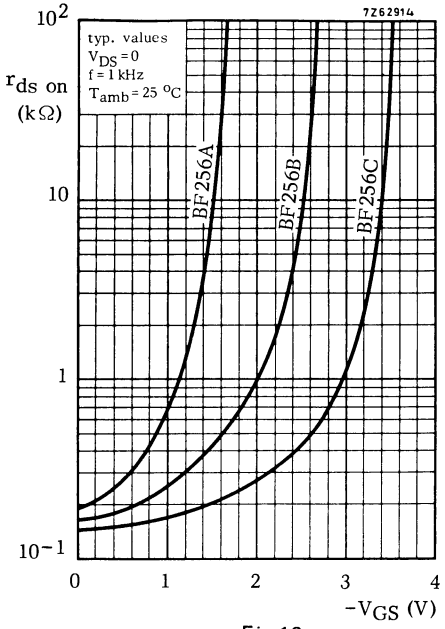


Fig. 16

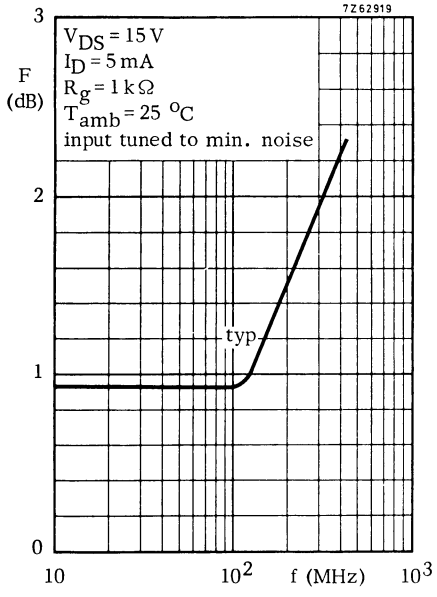


Fig. 17

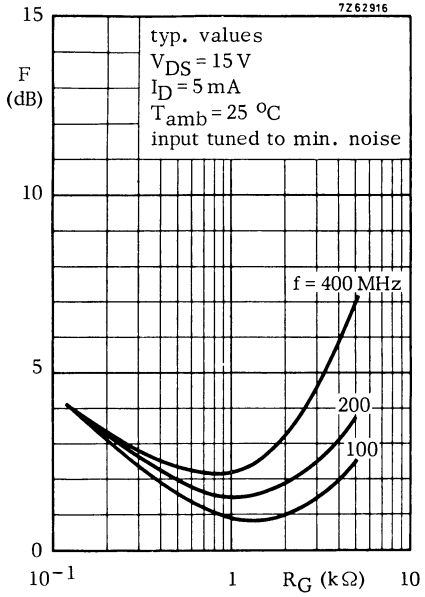


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the v.h.f. range.
These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

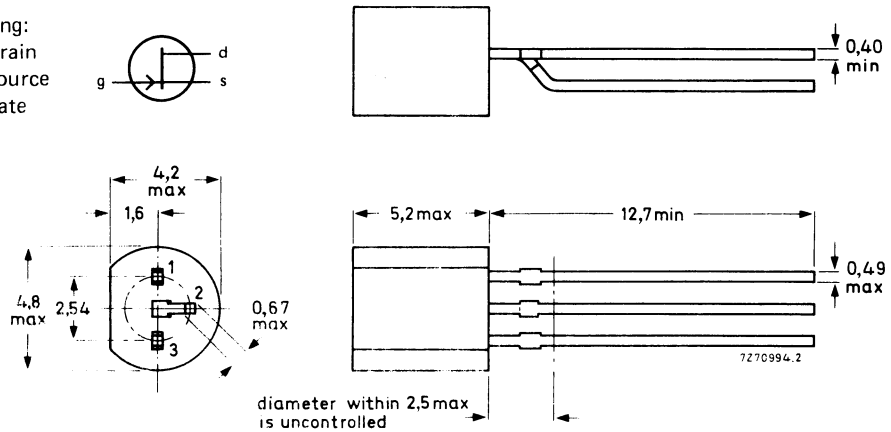
Drain-source voltage	V_{DS}	max.		20			V
Drain current (d.c. or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.		300			mW
			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0,3	0,3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0,3	0,3	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz V_{DS} = 10 V; V_{GS} = 0	F	typ.	1,5	1,5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1,5	1,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 0,2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and B
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and D

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0,3	0,3	0,3	0,3	pF
		<	0,4	0,4	0,4	0,4	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4,0	4,0	3,5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	>	–	–	6,0	7,0	mS
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3,5	5,5	5,0	5,0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

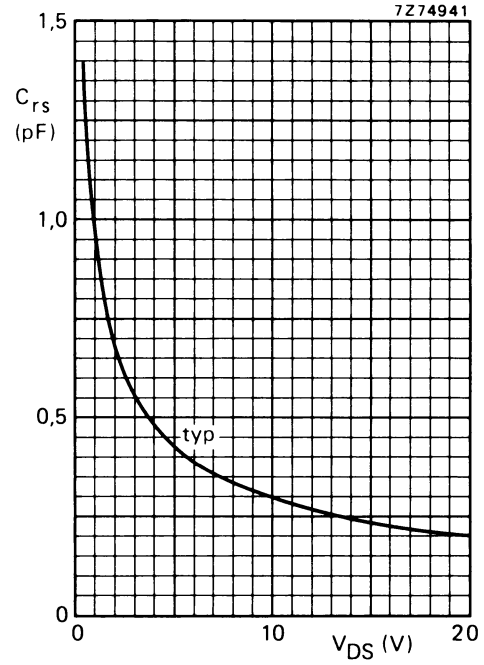


Fig. 2 V_{GS} = 0 for **BF410A** and **BF410B**; I_D = 5 mA for **BF410C** and **BF410D**; f = 1 MHz; T_{amb} = 25 °C.

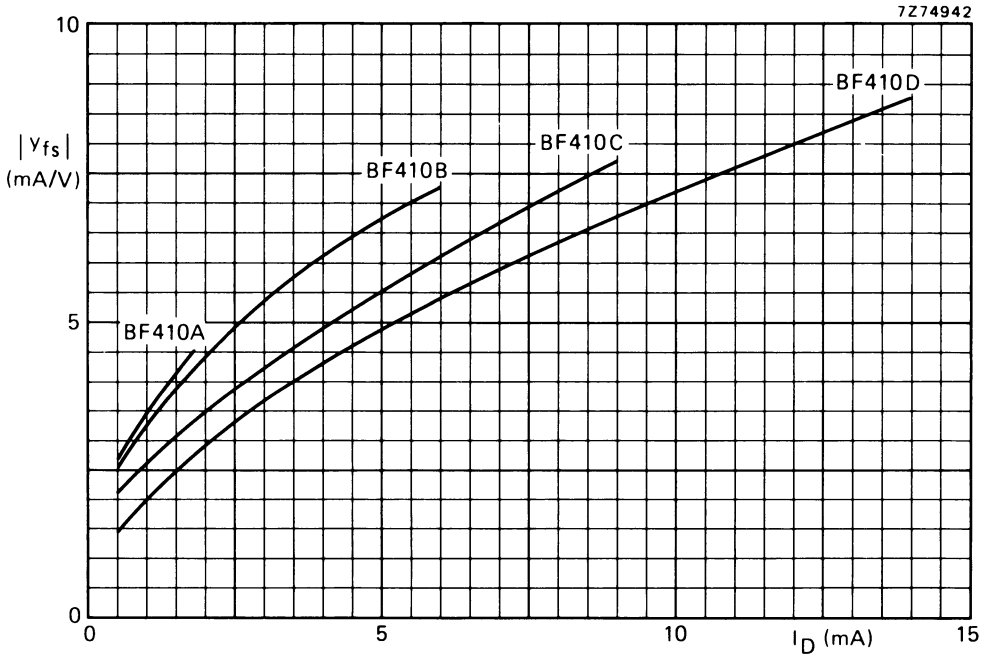


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.		20		V
Drain current (DC or average)	I_D	max.		30		mA
Total power dissipation up to $T_{amb} = 40\ ^oC$	P_{tot}	max.		250		mW
			BF510	511	512	513	
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Transfer admittance (common source) $V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2.5	4	6	7	mS
Feedback capacitance $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	0.3	0.3	–	–	pF
$V_{DS} = 10$ V; $I_D = 5$ mA	C_{rs}	typ.	–	–	0.3	0.3	pF
Noise figure at optimum source admittance $G_S = 1$ mS; $-B_S = 3$ mS; f = 100 MHz							
$V_{DS} = 10$ V; $V_{GS} = 0$	F	typ.	1.5	1.5	–	–	dB
$V_{DS} = 10$ V; $I_D = 5$ mA	F	typ.	–	–	1.5	1.5	dB

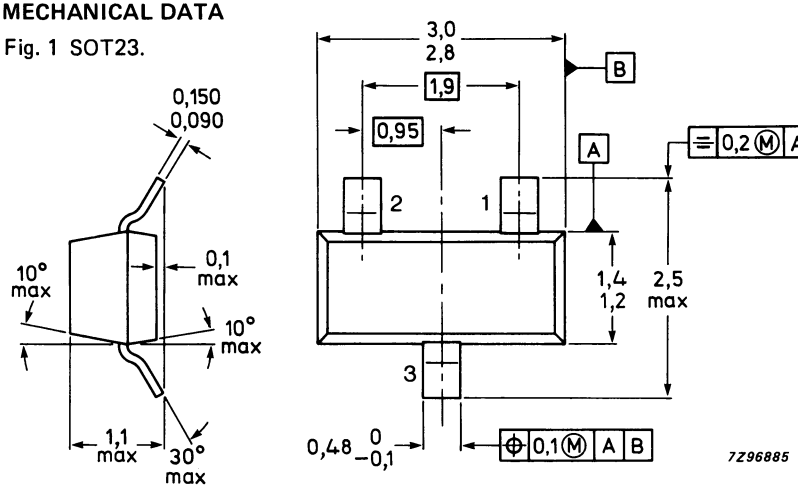
MECHANICAL DATA

SOT23.

See also *Soldering recommendations.*

MECHANICAL DATA

Fig. 1 SOT23.

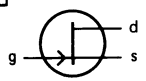


TOP VIEW

Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source



Marking code

BF510 = S6
BF511 = S7
BF512 = S8
BF513 = S9

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
→ Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250	mW
→ Storage temperature range	T_{stg}	−65 to +	150	°C
→ Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511

V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.3	0.3	0.3	0.3	pF
		<	0.4	0.4	0.4	0.4	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	>	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance							
G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

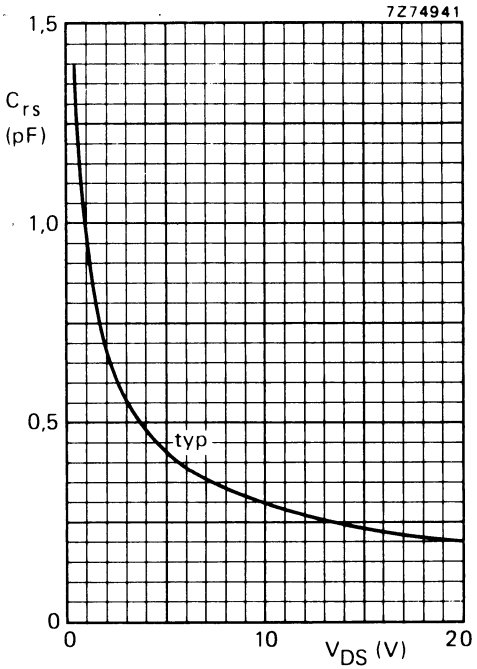


Fig. 2 V_{GS} = 0 for BF510 and BF511; I_D = 5 mA for BF512 and BF513; f = 1 MHz; T_{amb} = 25 °C.

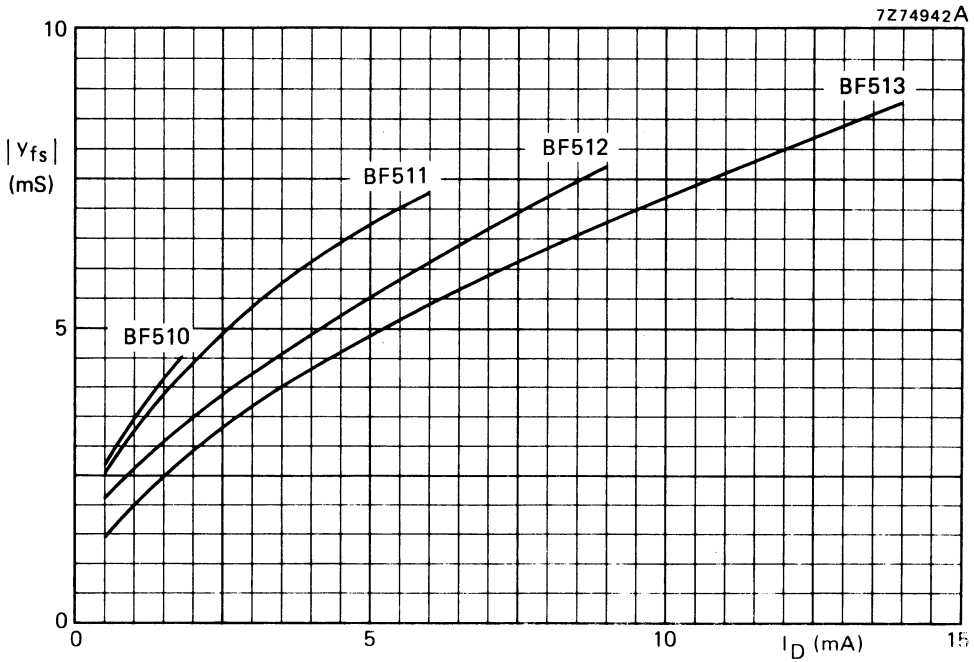


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

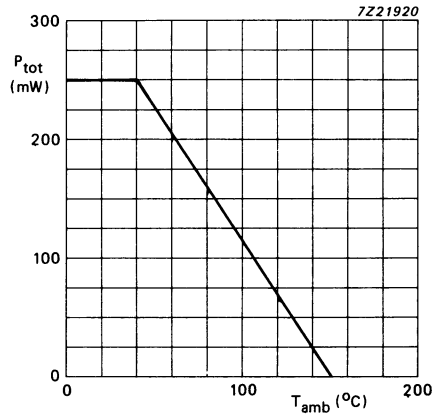


Fig.4 Power derating curve.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

		BFQ10	11	12	13	14	15	16	
Difference in gate current	$\lvert\Delta I_G\rvert$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	< 5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0.98 < 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.95 1.05	0.95 1.05	
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	< 18	30	40	50	60	70	100	μV/V ←
Common mode rejection ratio	CMRR	> 95	90	85	85	80	80	80	dB ←

MECHANICAL DATA

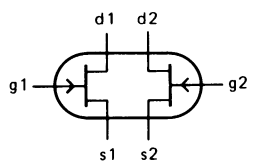
Dimensions in mm

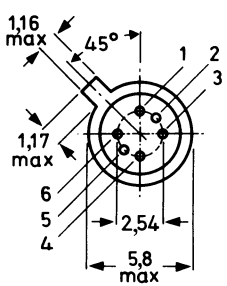
Fig. 1 TO-71.

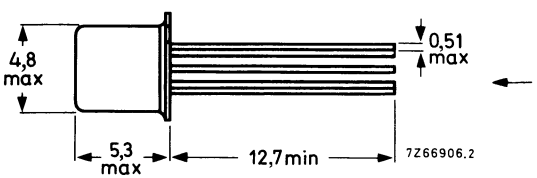
All leads insulated from the case.

Pinning

1 = source 1
2 = drain 1
3 = gate 1
4 = source 2
5 = drain 2
6 = gate 2







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

Measured at: I_D = 200 μA; V_{DG} = 15 V except for drain current ratio.

			BFQ10	11	12	13	14	15	16		
Drain current ratio (note 1) V_{DG} = 15 V; V_{GS} = 0	$\frac{I_{1D\text{-}1SS}}{I_{2D\text{-}2SS}}$	>	0.97	0.95	0.95	0.95	0.92	0.90	0.80		
		<	1.03	1.05	1.05	1.05	1.08	1.10	1.20		
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA	
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV	
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	5	5	10	20	20	40	50	μV/K	
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0.98	0.98	0.98	0.98	0.98	0.95	0.95		
		<	1.02	1.02	1.02	1.02	1.02	1.05	1.05		
Difference in transfer impedance (note 2)	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	6	6	12	12	12	20	30	Ω	
Difference in penetration factor (note 3)	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	18	30	40	50	60	70	100	μV/V	←
Common mode rejection ratio (note 4)	CMRR	>	95	90	85	85	80	80	80	dB	←

Notes

1. Measured under pulse conditions.
2. The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

   $\left(\Delta\frac{1}{g_{fs}} = \frac{d\Delta V_{GS}}{dI_D}\right.$ at V_{DG} = constant).
3. The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

   $\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\Delta V_{GS}}{dV_{DG}}\right.$ at I_D = constant).
4. Common mode rejection ratio:

   CMRR (in dB) = $-20\log\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$.

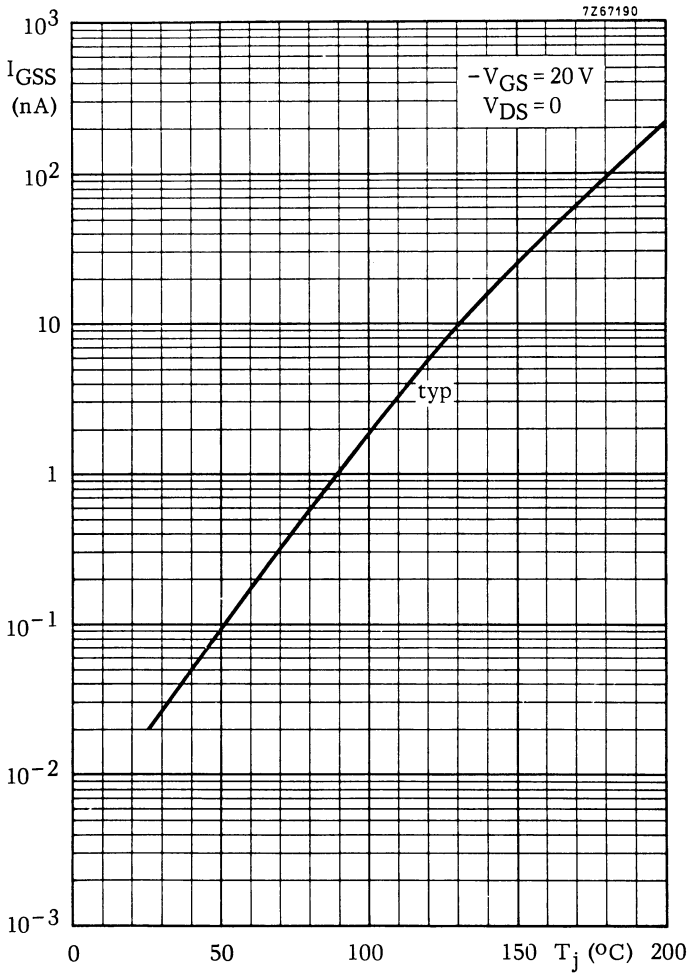
CHARACTERISTICS (Individual transistor)

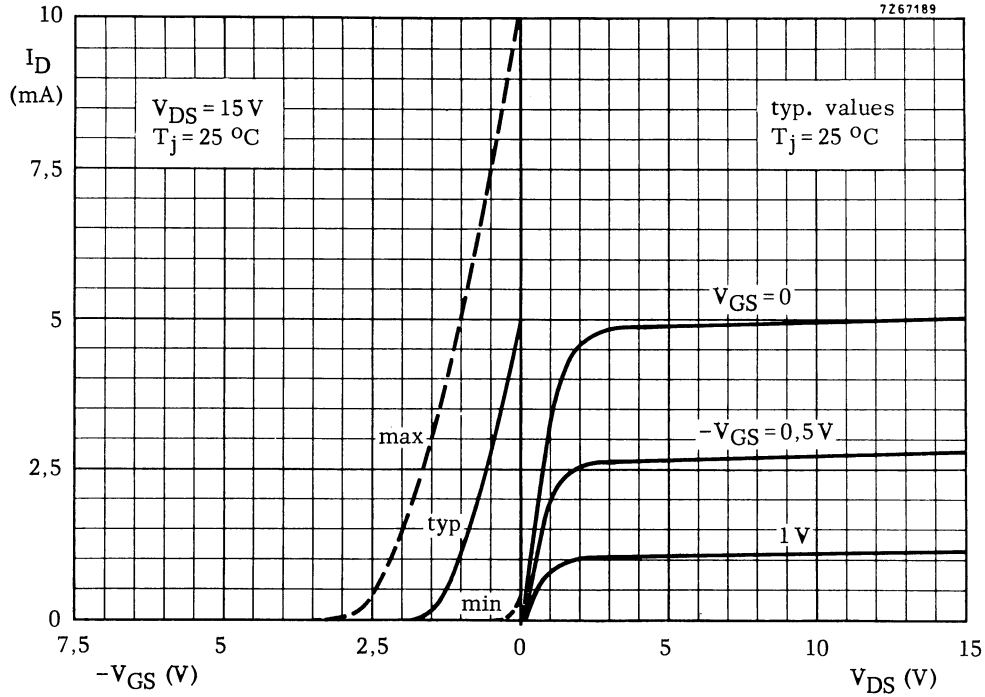
T_{amb} = 25 °C unless otherwise specified

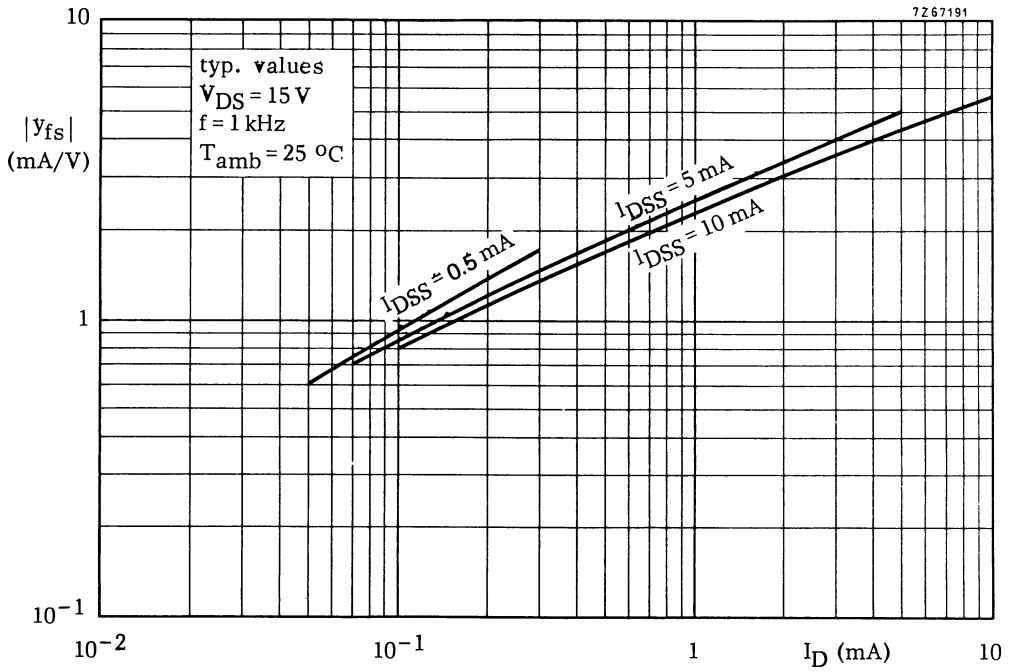
Gate cut-off current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100 pA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20 nA
Gate current			
I_D = 200 μA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10 nA
Drain current (note 1)			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		0.5 to 10 mA
Gate-source voltage			
I_D = 200 μA; V_{DG} = 15 V	$-V_{GS}$	<	2.7 V
Gate-source cut-off voltage			
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$		0.5 to 3.5 V
Transfer conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{os}	<	5 μS
Input capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{is}	<	8 pF
Feedback capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{rs}	<	1.0 pF
Equivalent noise voltage			
I_D = 200 μA; V_{DS} = 15 V; B = 0.6 to 100 Hz	V_n	<	0.5 μV

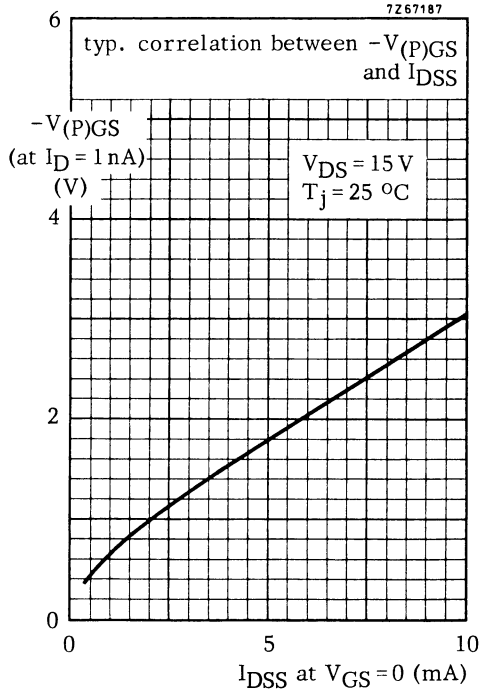
Notes

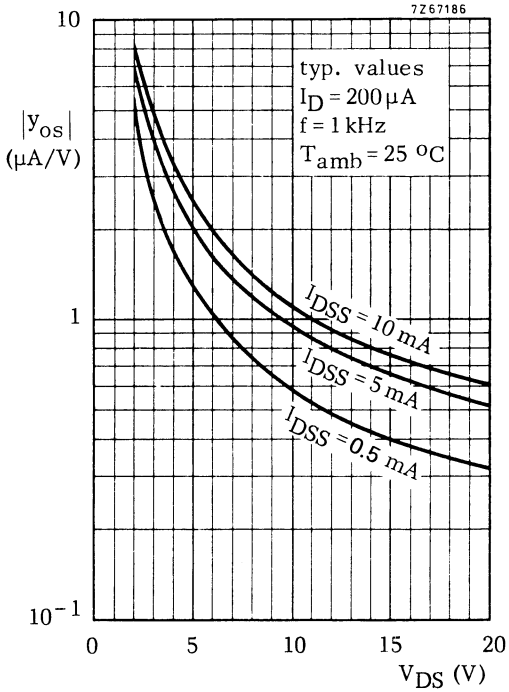
1. Measured under pulse conditions.
2. Measured with case grounded.

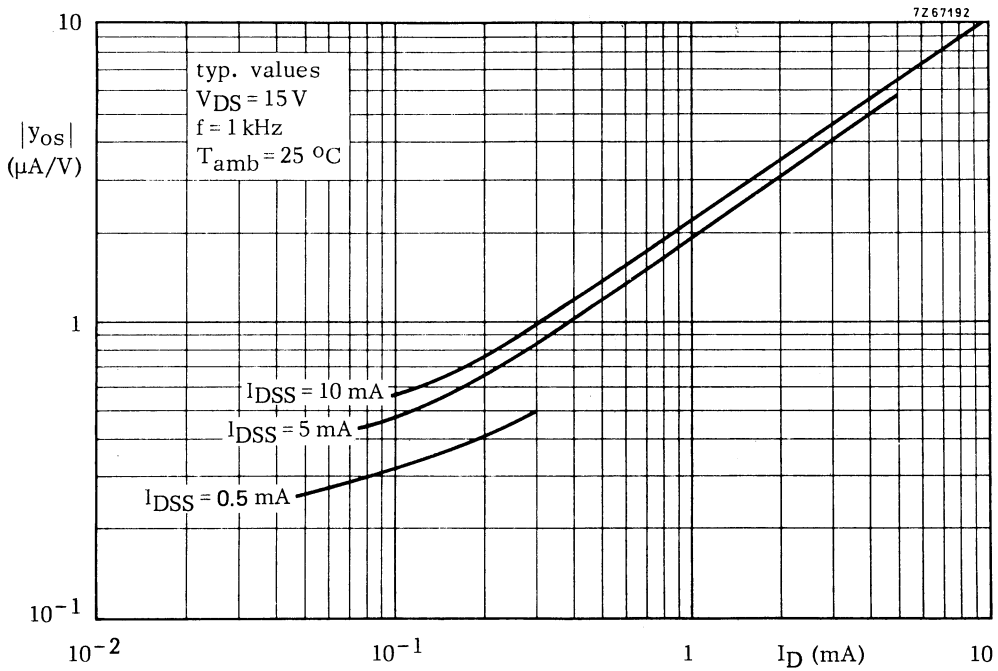

7Z67190
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 20$ V
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

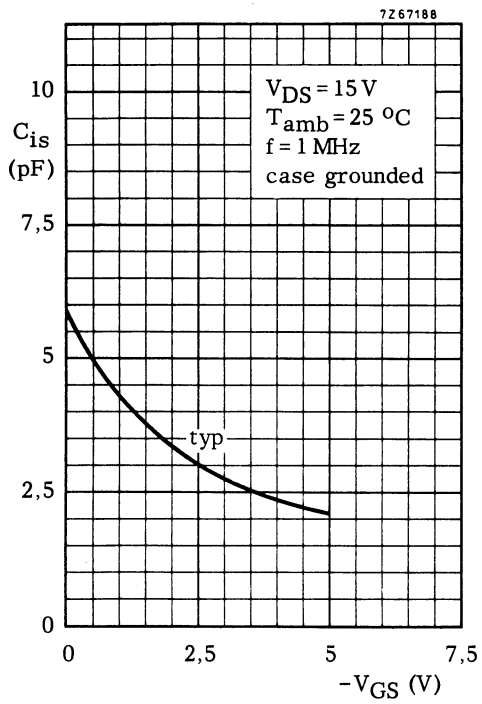

7Z67189
10
I_D (mA)
7,5
5
2,5
0
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
max
typ
min
7,5
5
2,5
0
5
10
15
$-V_{GS}$ (V)
V_{DS} (V)

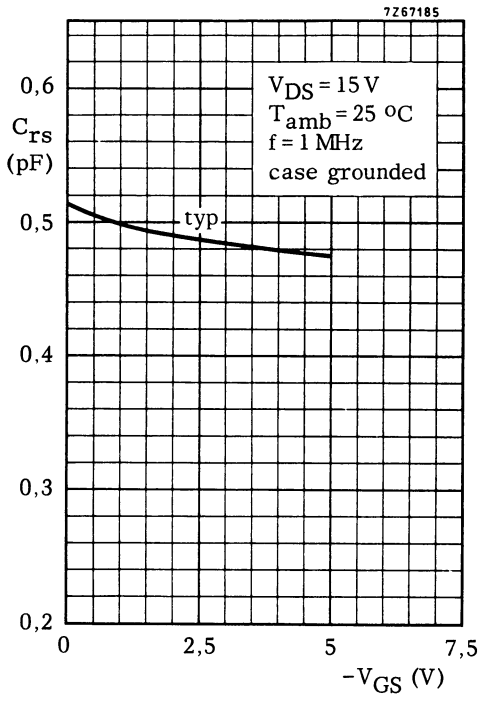

7Z67191
10
$|y_{fs}|$ (mA/V)
1
10^{-1}
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
I_{DSS} = 0.5 mA
I_{DSS} = 5 mA
I_{DSS} = 10 mA
10^{-2}
10^{-1}
1
I_D (mA)
10

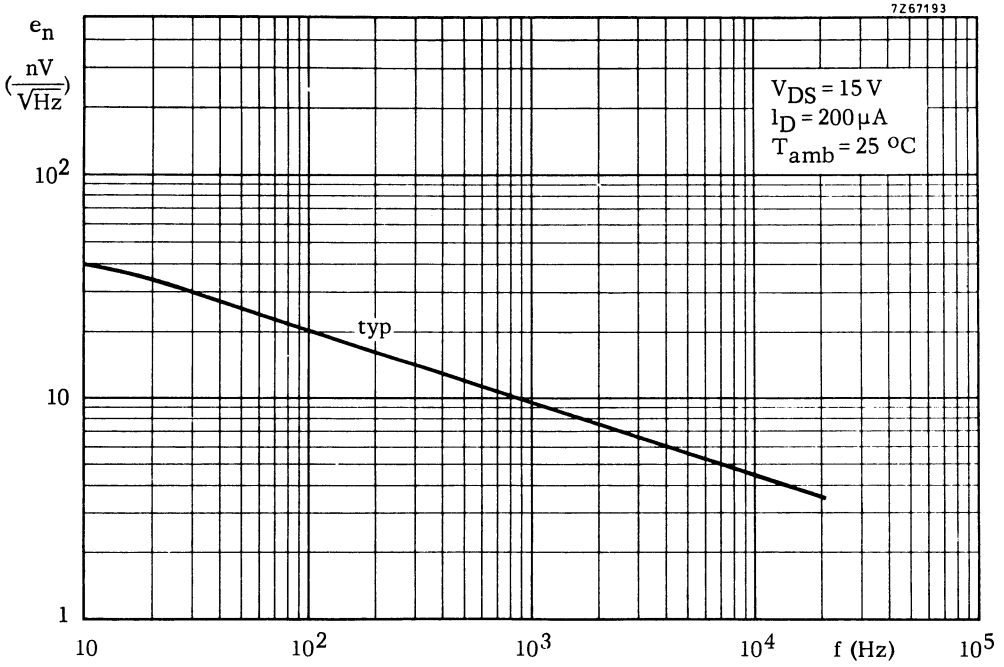

7Z67187
typ. correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ (at I_D = 1 nA) (V)
V_{DS} = 15 V
T_j = 25 °C
6
4
2
0
0
5
10
I_{DSS} at V_{GS} = 0 (mA)


7Z67186
typ. values
I_D = 200 µA
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0.5 mA
10
1
10^{-1}
0
5
10
15
20
V_{DS} (V)


7Z67192
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0.5 mA
10
1
10^{-1}
10^{-2}
10^{-1}
1
I_D (mA)
10


7Z67188
10
C_{is} (pF)
7,5
5
2,5
0
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67185
0,6
C_{rs} (pF)
0,5
0,4
0,3
0,2
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67193
e_n ($\frac{nV}{\sqrt{Hz}}$)
10^2
10
1
V_{DS} = 15 V
I_D = 200 µA
T_{amb} = 25 °C
typ
10
10^2
10^3
10^4
f (Hz)
10^5

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

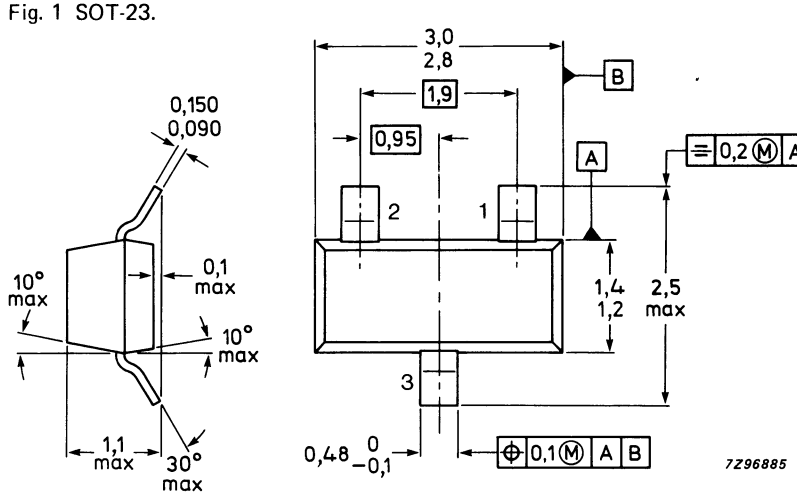
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250		mW
			BFR30	BFR31	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Transfer admittance (common source) I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz	$\|y_{fs}\|$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



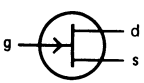
TOP VIEW

Marking code

BFR30 = M1
BFR31 = M2

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
→ Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250	mW
→ Storage temperature range	T_{stg}		−65 to + 150	°C
→ Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFR30	BFR31	
Gate cut-off current					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	max.	0.2	0.2	nA
Drain current					
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Gate-source voltage					
I_D = 1 mA; V_{DS} = 10 V	$-V_{GS}$	min.	0.7	0	V
		max.	3.0	1.3	V
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	max.	4.0	2.0	V
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	max.	5	2.5	V
y parameters					
Transfer admittance at f = 1 kHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	0.5	0.75	mS
Output admittance at f = 1 kHz					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	40	25	μS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	20	15	μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V B = 0.6 to 100 Hz	V_n	max.	0.5	0.5	μV

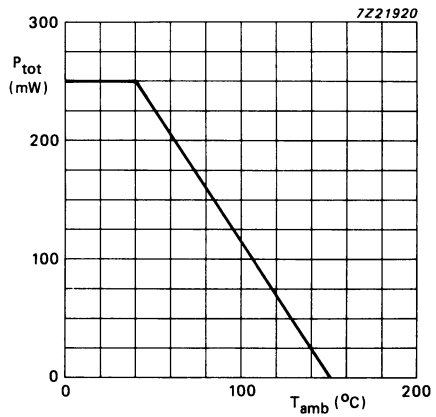


Fig.2 Power derating curve.

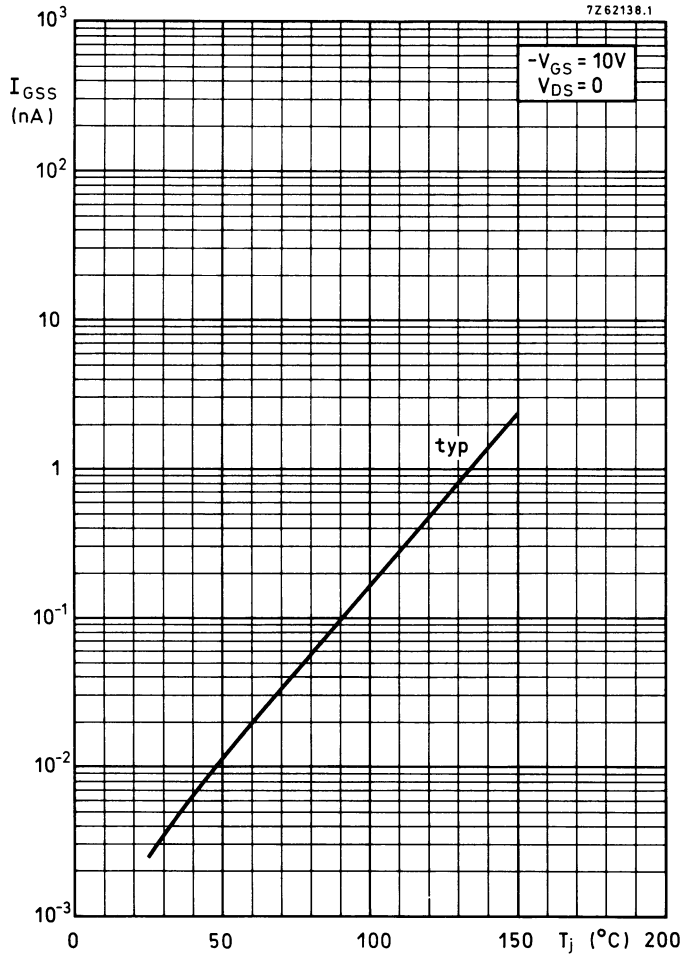

7Z62138.1
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

Fig.3.

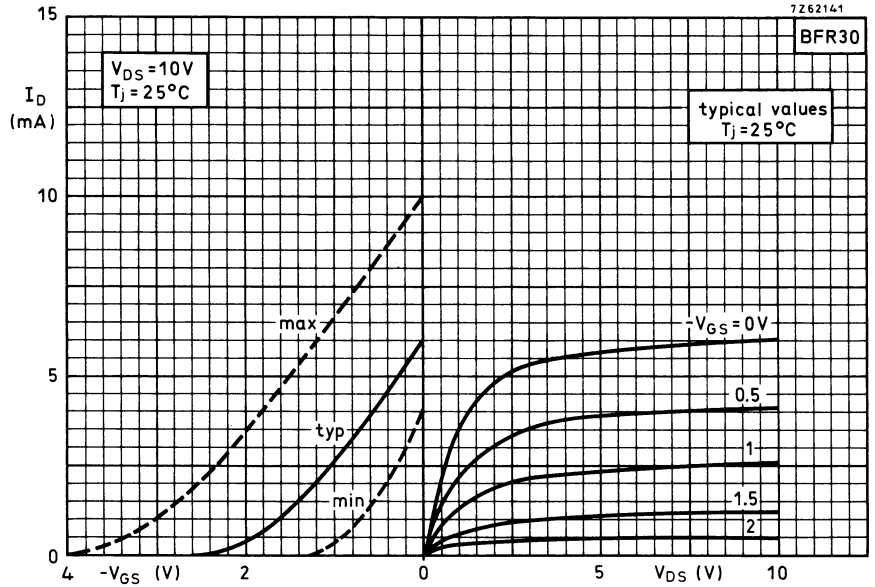

7Z62141
BFR30
V_{DS} = 10V
T_j = 25°C
typical values
T_j = 25°C
I_D
(mA)
15
10
5
0
max
typ
min
$-V_{GS}$ = 0V
0.5
1
1.5
2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.4.

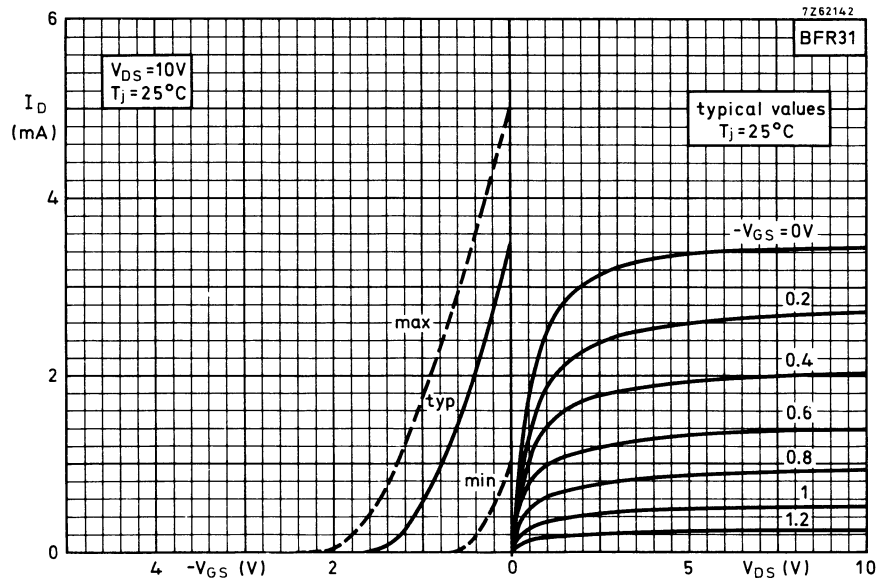

7Z62142
BFR31
V_{DS} = 10V
T_j = 25°C
typical values
T_j = 25°C
I_D
(mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
1
1.2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.5.

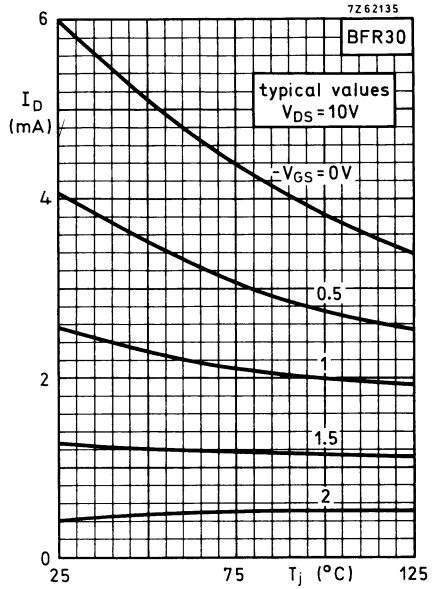


Fig.6.

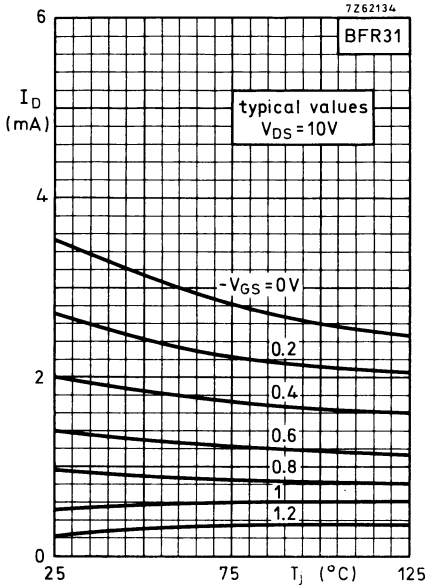


Fig.7.

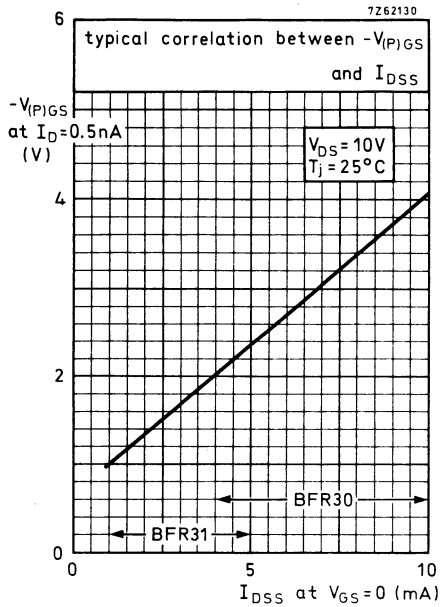


Fig.8.

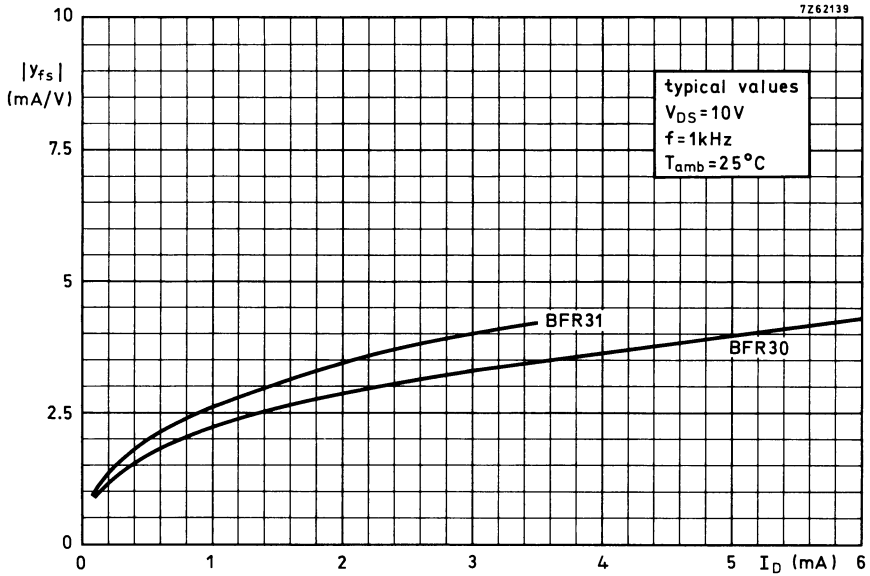

7Z62139
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR31
BFR30
0
1
2
3
4
5
ID (mA)
6

Fig.9.

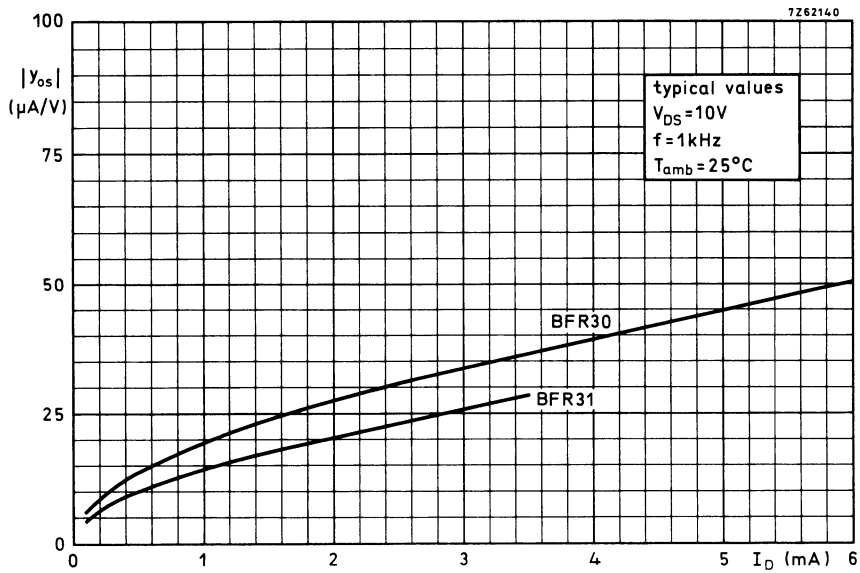

7Z62140
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR30
BFR31
0
1
2
3
4
5
ID (mA)
6

Fig.10.

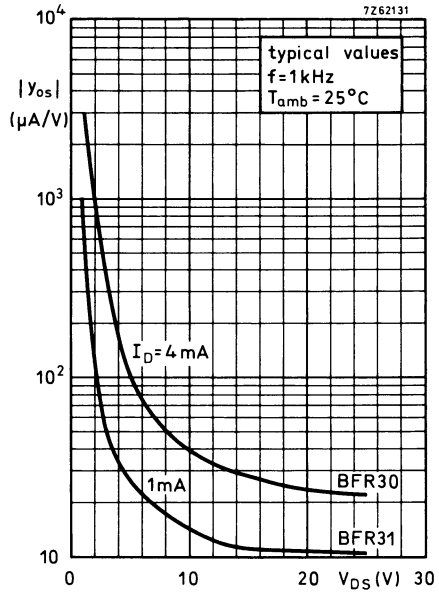


Fig.11.

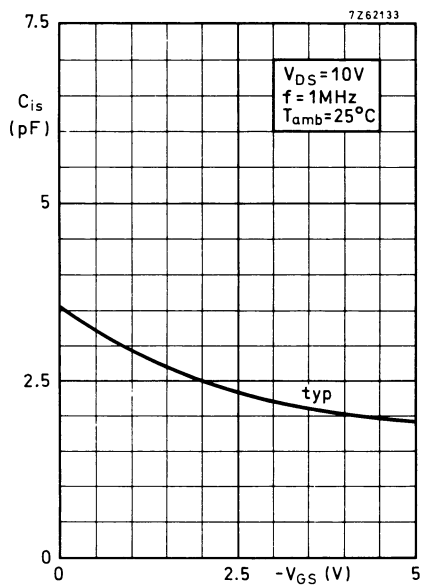


Fig.12.

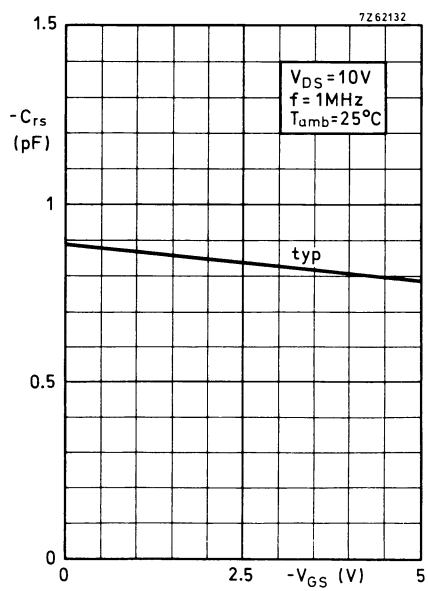


Fig.13.

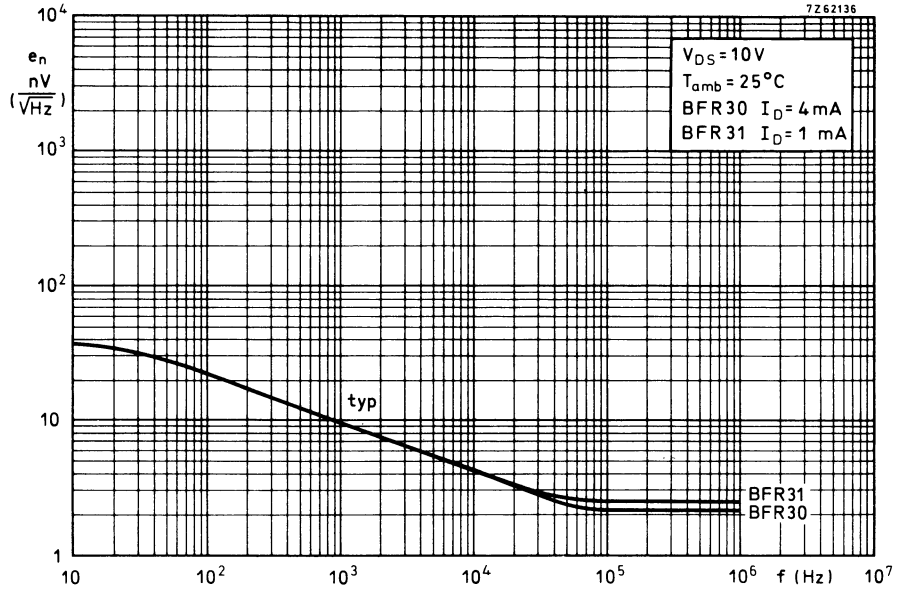

7Z62136
10^4
e_n
nV
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 10 V
T_{amb} = 25 °C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.14.

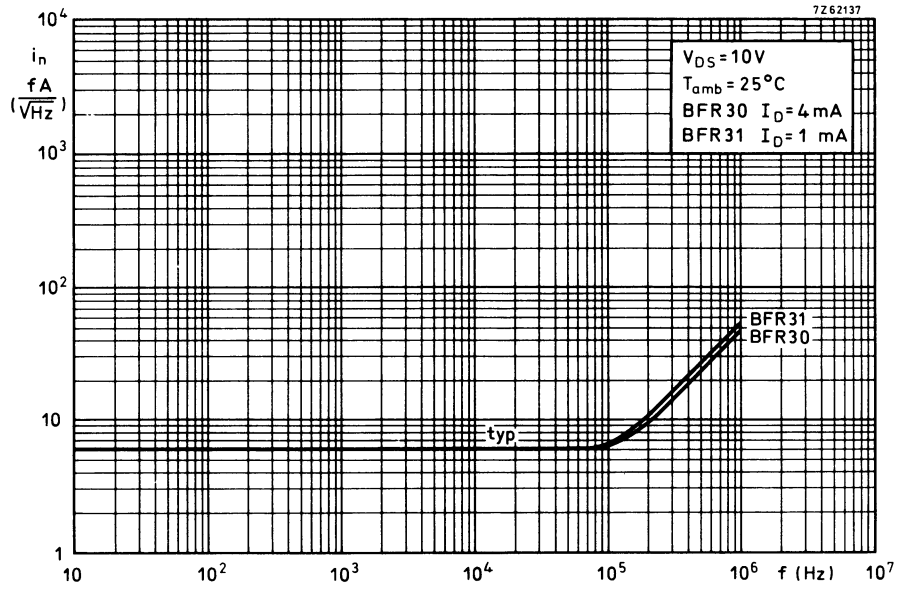

7Z62137
10^4
i_n
fA
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 10 V
T_{amb} = 25 °C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
BFR31
BFR30
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.15.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

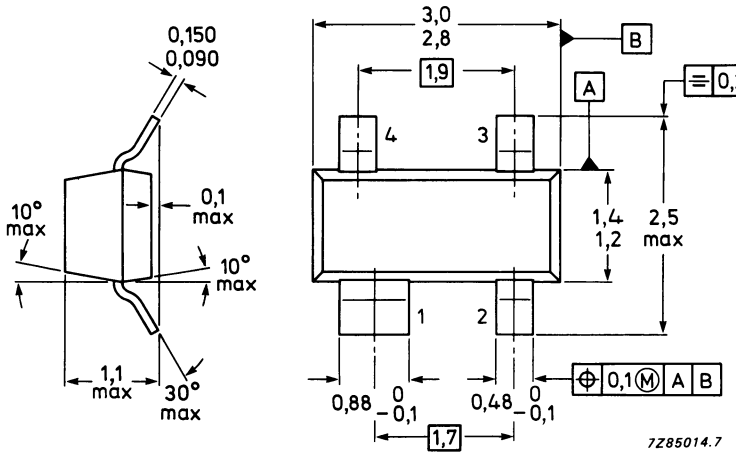
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30 V
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Drain current			
V_{DS} = 6 V; V_{GS} = 0: BFR101A	I_{DSS}		0,2 to 1,5 mA
V_{DS} = 6 V; V_{GS} = 0: BFR101B	I_{DSS}		1,0 to 5,0 mA
Transfer admittance (common source)			
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101A	$\lvert y_{fs} \rvert$	>	1,2 mS
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101B	$\lvert y_{fs} \rvert$	>	2,5 mS

MECHANICAL DATA

Fig. 1 SOT-143.

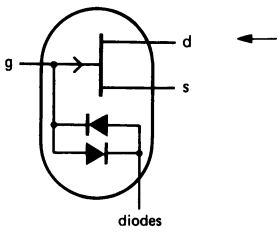
Dimensions in mm



TOP VIEW

Marking code

BFR101A = M97
BFR101B = M98



Pinning

1 = gate
2 = diodes
3 = source
4 = drain

Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current (d.c.)	I_D	max.	20	mA
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460	K/W

CHARACTERISTICS with source connected to case for all measurements

T_j = 25 °C unless otherwise specified

		BFR101A	BFR101B	
Gate leakage current				
V_{DS} = 6 V; I_D = 10 μA	$-I_G$	< 5	5	nA
Drain current				
V_{DS} = 6 V; V_{GS} = 0	I_{DSS}	0,2 to 1,5	1 to 5	mA
Gate-source cut-off voltage				
V_{DS} = 6 V; I_D = 1 μA	$-V_{(P)GS}$	0,2 to 1	0,5 to 2,5	V
Small-signal common-source characteristics				
V_{DS} = 6 V; V_{GS} = 0, T_{amb} = 25 °C				
Transfer admittance				
f = 1 kHz	$\lvert y_{fs}\rvert$	> 1,2	2,5	mS
Output admittance at f = 1 kHz	$\lvert y_{os}\rvert$	typ. 10	50	mS
Input capacitance at f = 1 MHz				
diodes not connected	C_{is}	< 5	5	pF
Diode capacitance				
V_D = 0; source and drain not connected	C_d	typ. 0,7	0,7	pF
Diode forward voltage				
± I_F = 10 mA	V_F	0,7 to 1,2	0,7 to 1,2	V

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7,5	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA

SOT-52 (see next page)

TOTAL DEVICE

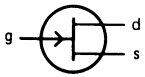
Dimensions in mm

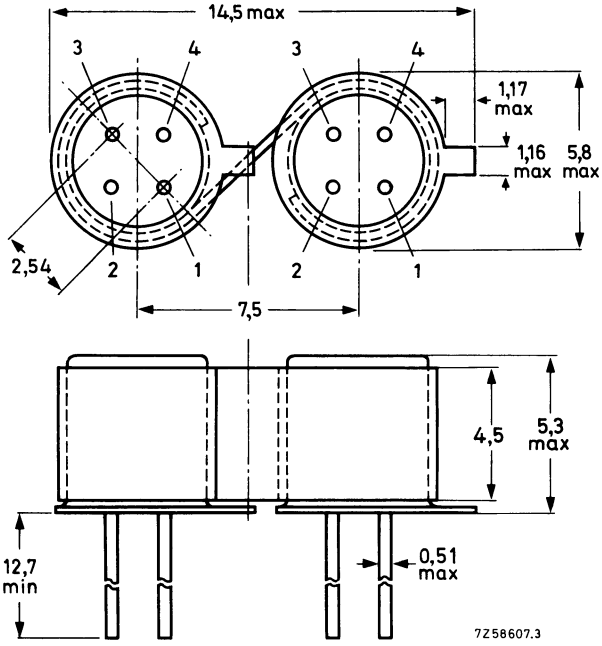
MECHANICAL DATA

SOT52

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case





Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}	−20 to + 100	°C

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

			BFS21	BFS21A	
Drain current ratio					
V_{DG} = 15 V; V_{GS} = 0; T_j = 25 °C	$\frac{I_{D1\text{-}S1S}}{I_{D2\text{-}S2S}}$	>	0.95	0.95	
		<	1.05	1.05	
Gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Change of gate-source voltage difference with ambient temperature					
T_{amb} = 25 to 100 °C					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
Difference of penetration factors*					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
Difference of transfer impedances**					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7.8	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	75	37.5	Ω

* The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,V_{DG}} \text{ at } I_D = \text{constant}\right)$$

** The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta\frac{1}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,I_D} \text{ at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

			BFS21	BFS21A	
Common mode rejection ratio*					
I_D = 500 μA; V_{DG} = 15 V	CMRR	>	60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	>	60	66	dB

INDIVIDUAL TRANSISTOR

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25°C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Junction temperature	T_j	max.	200	°C

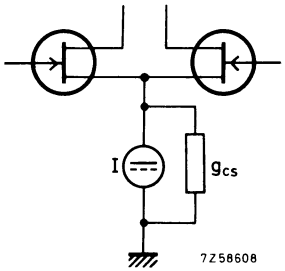
THERMAL RESISTANCE

From junction to ambient in free air (for individual transistor without S-clip)	$R_{th\ j\text{-}a}$	=	590	K/W

→ * **Common mode rejection ratio**

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \tfrac{1}{2}\, g_{cs}\, \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.



The guaranteed values of CMRR apply at g_{cs} = 0.1 μΩ^{-1}

CHARACTERISTICS (individual transistor)

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
I_D = 500 μA; V_{DS} = 15 V	I_G	<	0.5 nA
I_D = 500 μA; V_{DS} = 15 V; T_{amb} = 100 °C	I_G	<	25 nA
Drain current			
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C	I_{DSS}	>	1 mA
Gate-source cut-off voltage			
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	6 V
Transfer conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{os}	<	15 μS
Input capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{rs}	<	0.75 pF
Equivalent noise voltage			
f = 10 Hz			
I_D = 500 μA; V_{DS} = 15 V	$V_n/\sqrt{B}$	<	200 nV/$\sqrt{Hz}$
V_{DS} = 15 V; V_{GS} = 0	$V_n/\sqrt{B}$	<	75 nV/$\sqrt{Hz}$

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

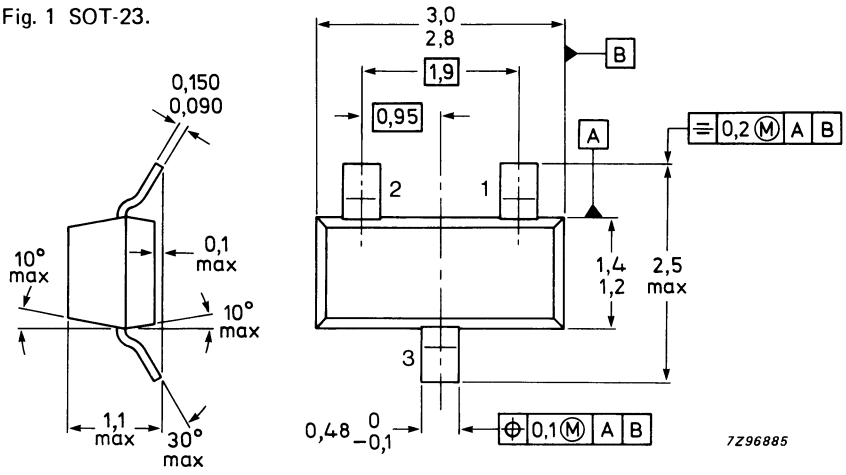
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,2 1,5	mA mA
Transfer admittance (common source) I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	mS
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	<	0,5	μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



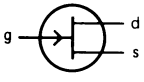
TOP VIEW

Marking code

BFT46 = M3

Pinning

1 = drain
2 = source
3 = gate



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
→ Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250 mW
→ Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

→ From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2 nA
Drain current			
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2 mA
		<	1,5 mA
Gate-source voltage			
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1 V
		<	1,0 V
Gate-source cut-off voltage			
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2 V
y-parameters at f = 1 kHz;			
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	1,0 mS
Output admittance	$\lvert y_{os} \rvert$	<	10 μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	0,5 mS
Output admittance	$\lvert y_{os} \rvert$	<	5 μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	<	0,5 μV

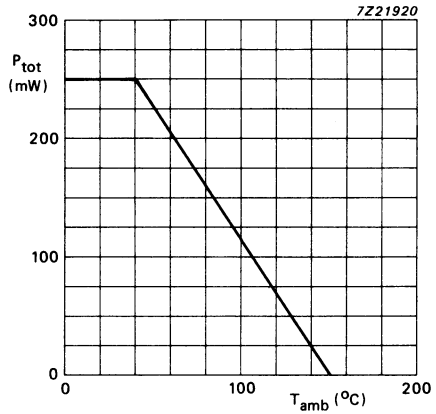


Fig.2 Power derating curve.

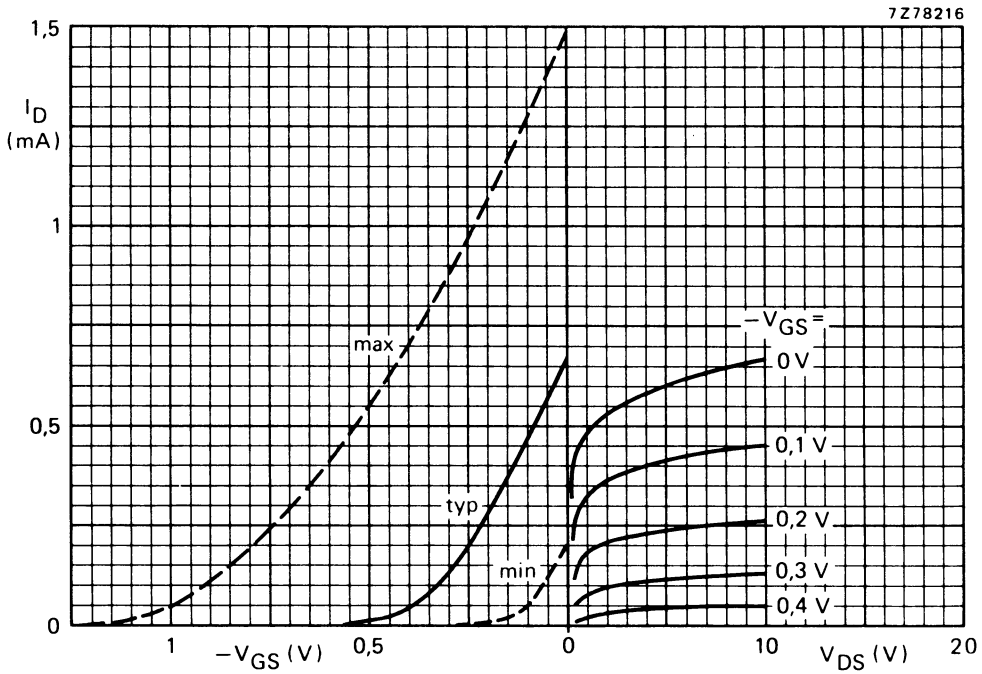


Fig. 3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

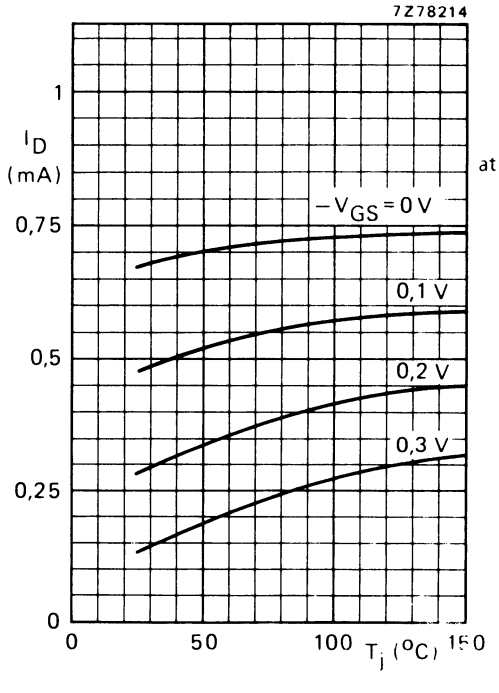


Fig. 4 Typical values. V_{DS} = 10 V.

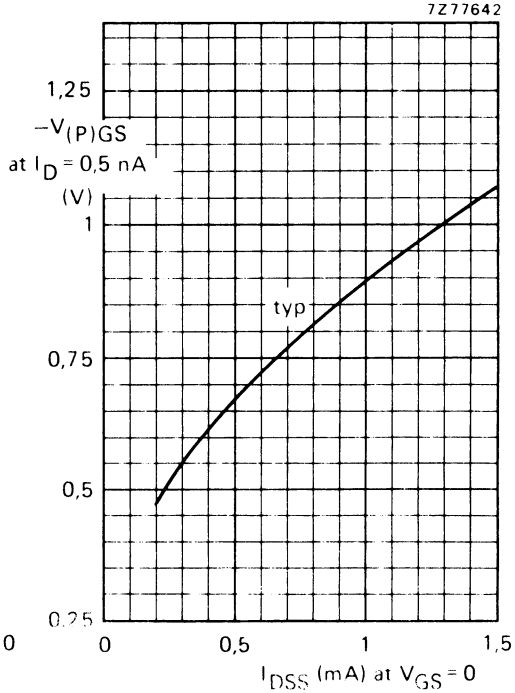


Fig. 5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

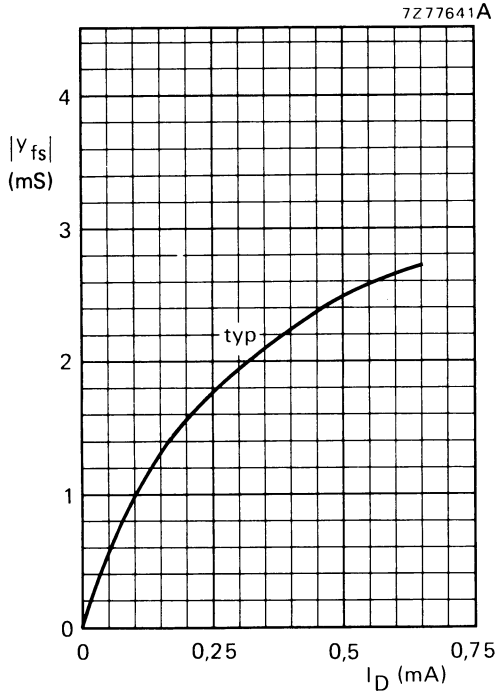


Fig. 6

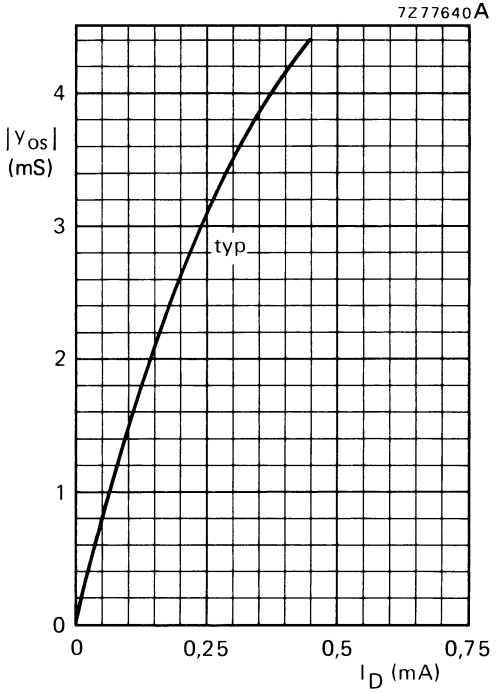


Fig. 7

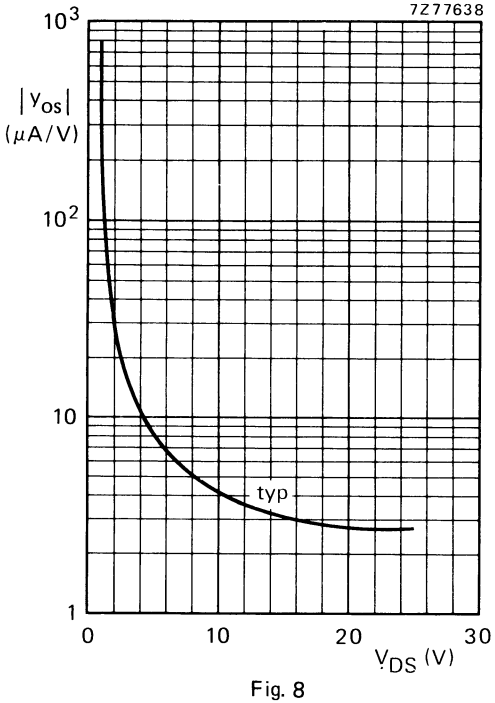


Fig. 8

Fig. 6 $|y_{fs}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 7 $|y_{os}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 8 $|y_{os}|$ versus V_{DS}.
I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

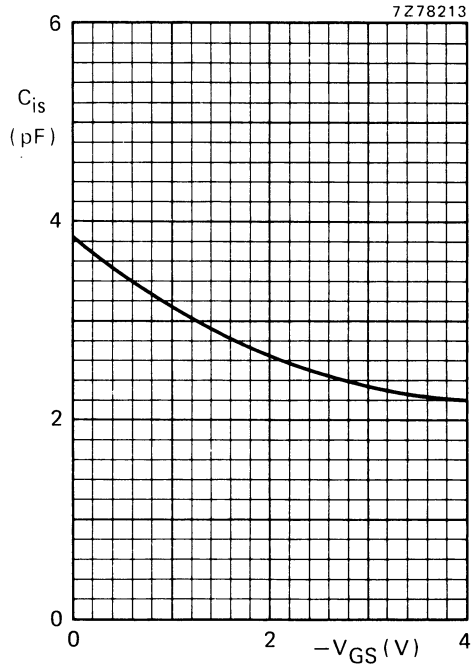


Fig. 9

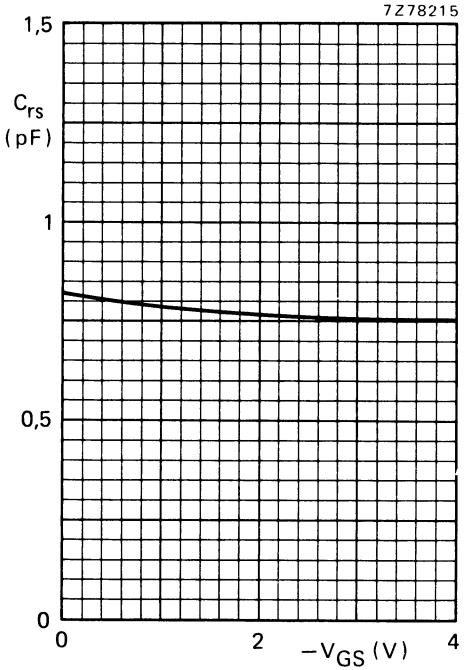


Fig. 10

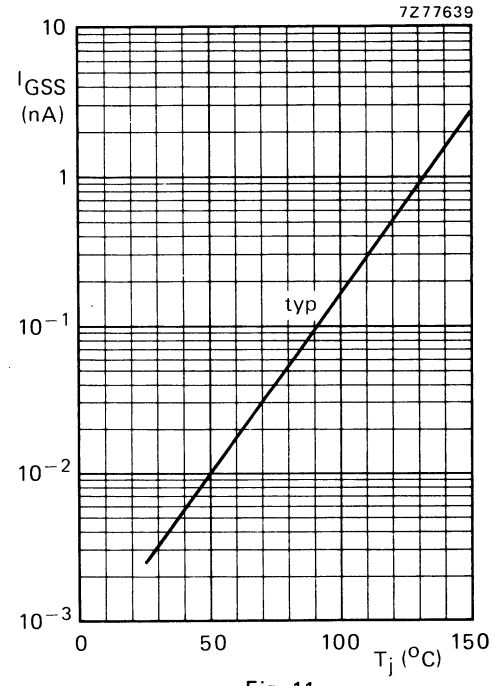


Fig. 11

Fig. 9 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 11 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

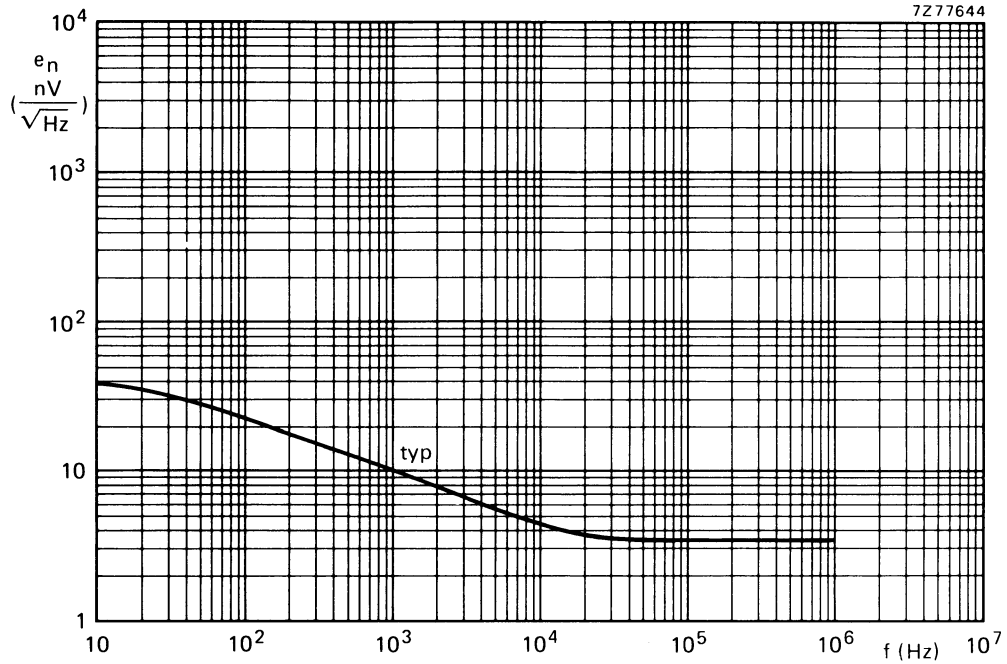


Fig. 12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

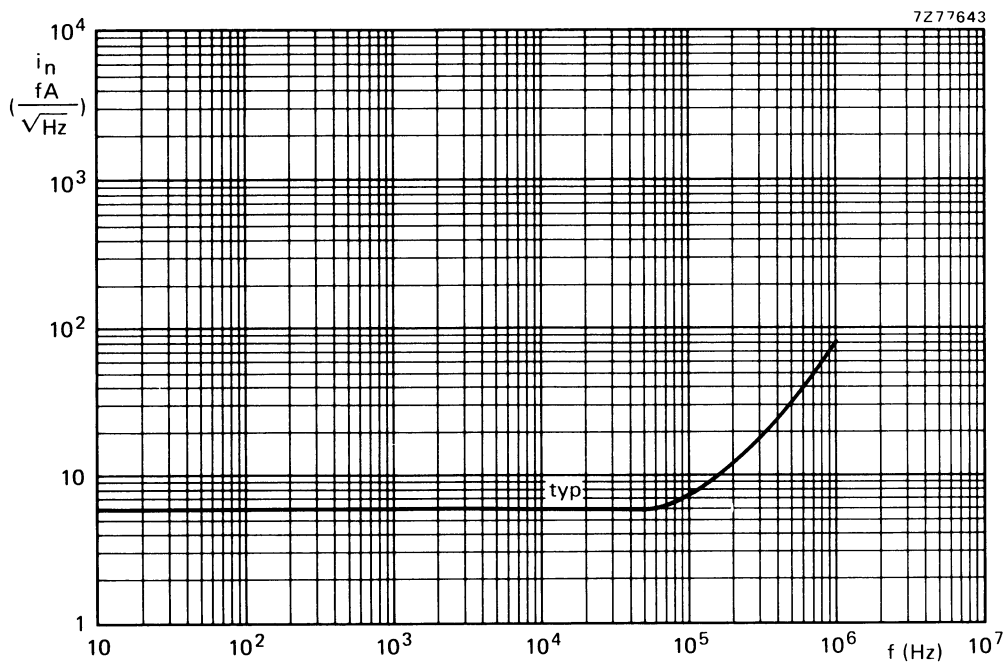


Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300		mW
			BFW10	**BFW11**	
Drain current		>	8	4	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	20	10	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	3,2	mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0					
f = 100 MHz; R_G = 1 kΩ	F	<	2,5	2,5	dB
Equivalent noise voltage					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

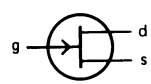
MECHANICAL DATA

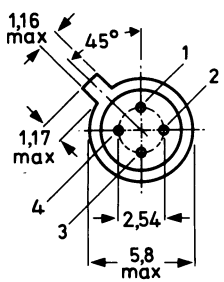
Dimensions in mm

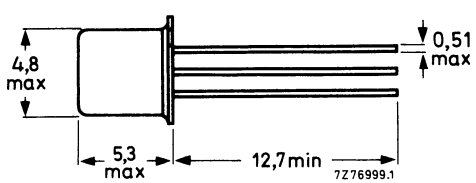
Fig.1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Storage temperature	T_{stg}	−65 to +	200 °C
Junction temperature	T_j	max.	200 °C

THERMAL RESISTANCE

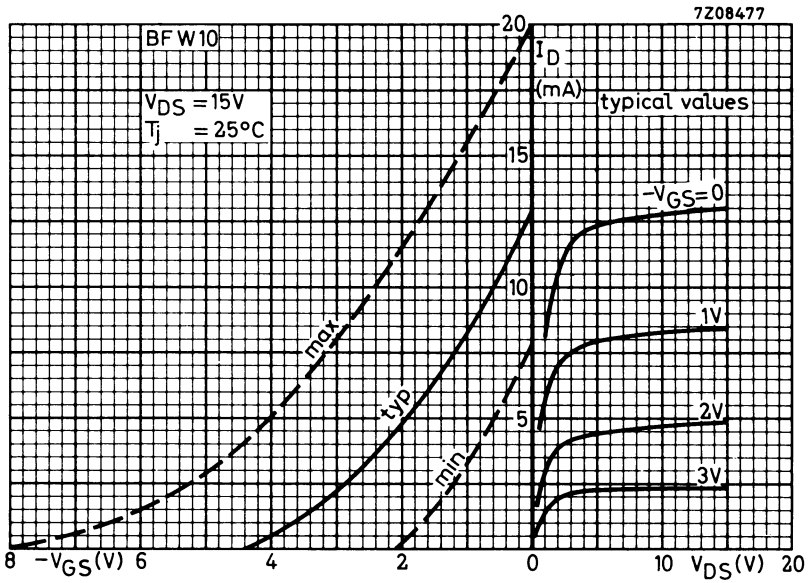
From junction to ambient	$R_{th\ j\text{-}a}$	=	590 K/W

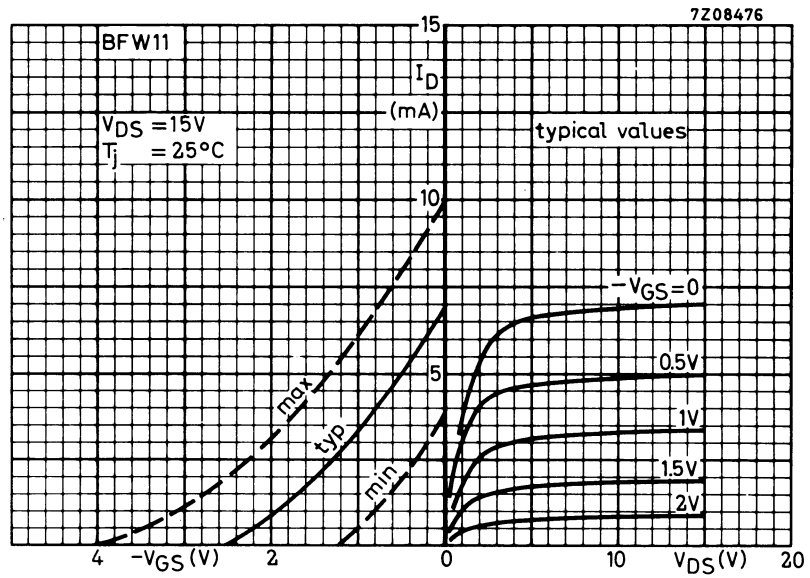
CHARACTERISTICS

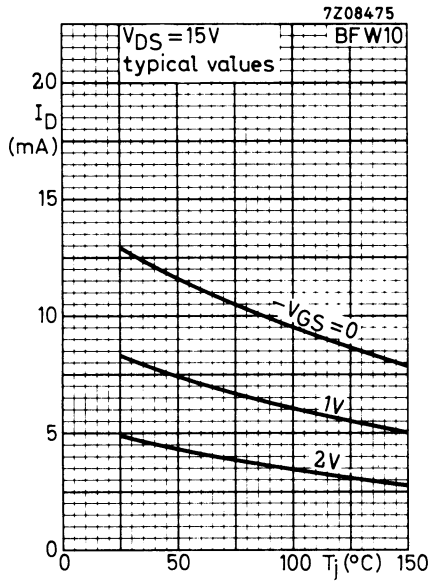
T_j = 25 °C unless otherwise specified

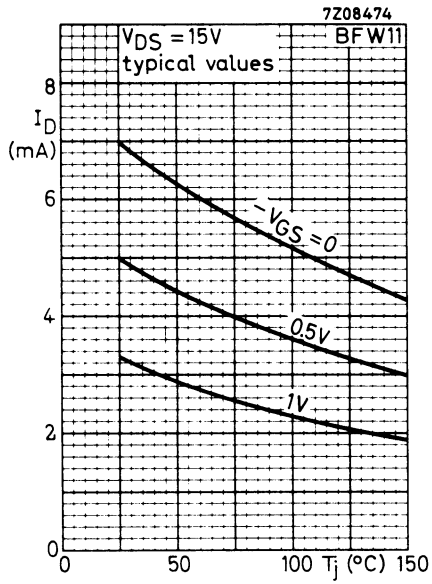
			BFW10	BFW11	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current*					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 1 kHz					
Transfer admittance	$\lvert y_{fs} \rvert$	>	3.5	3.0	mS
		<	6.5	6.5	mS
Output admittance	$\lvert y_{os} \rvert$	<	85	50	μs
f = 1 MHz; input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz; transfer admittance	$\lvert y_{fs} \rvert$	>	3.2	3.2	mS
Input capacitance	g_{is}	<	800	800	μS
Output capacitance	g_{os}	<	200	100	μS
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

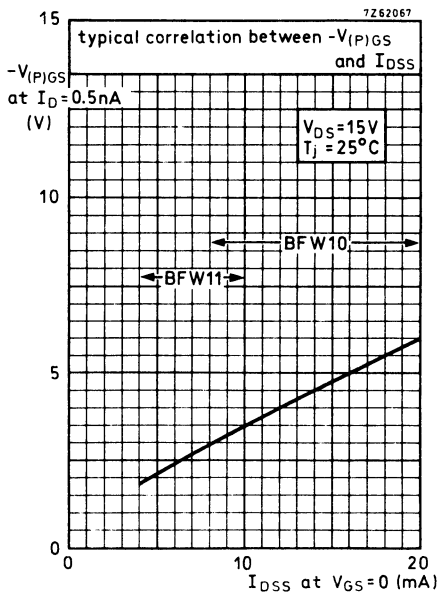
* Measured under pulsed conditions.

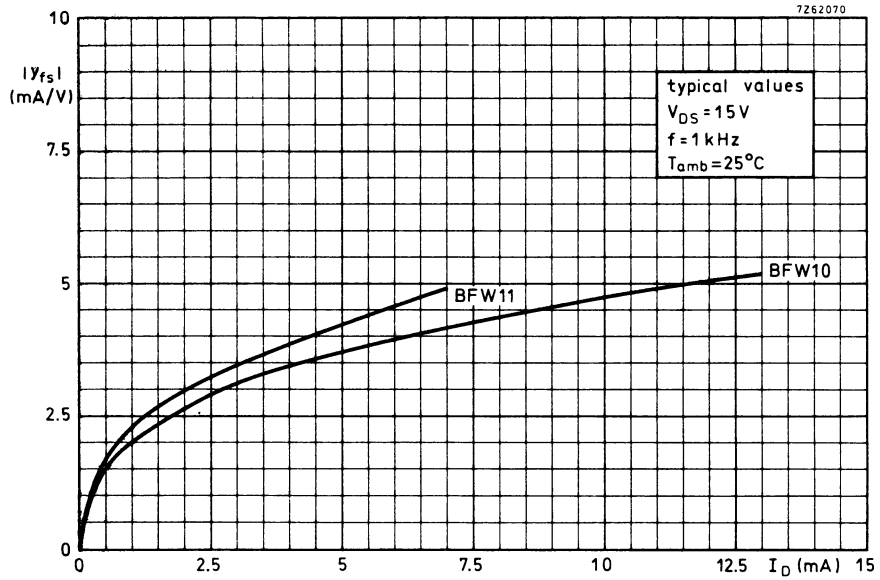

7Z08477
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
20
15
10
5
8
6
4
2
0
10
20
$-V_{GS}$(V)
V_{DS}(V)

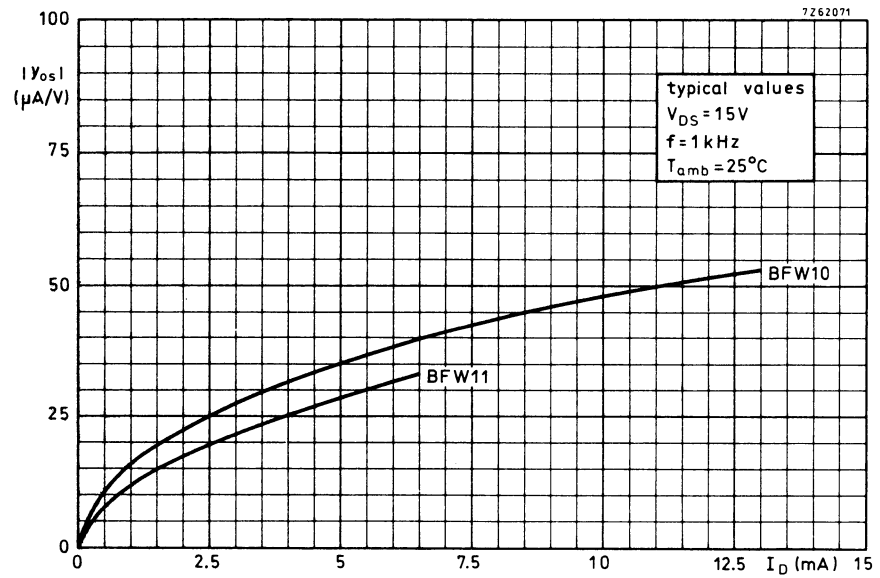

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
15
10
5
4
2
0
10
20
$-V_{GS}$(V)
V_{DS}(V)

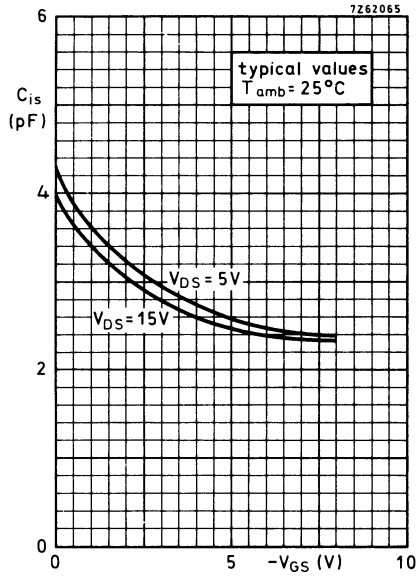

7Z08475
V_{DS} = 15V
typical values
BFW10
I_D (mA)
20
15
10
5
0
$-V_{GS}$ = 0
1V
2V
0
50
100
T_j (°C)
150

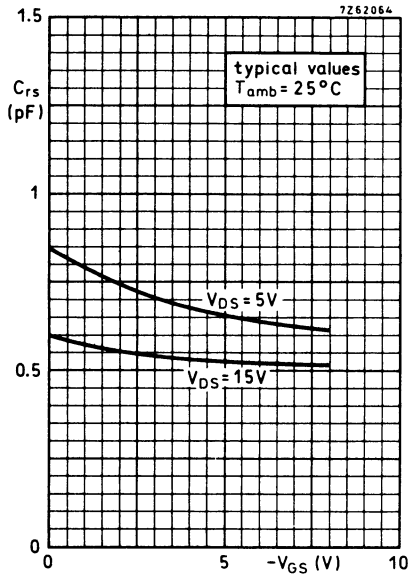

7Z08474
V_{DS} = 15V
typical values
BFW11
I_D (mA)
8
6
4
2
0
$-V_{GS}$ = 0
0.5V
1V
0
50
100
T_j (°C)
150

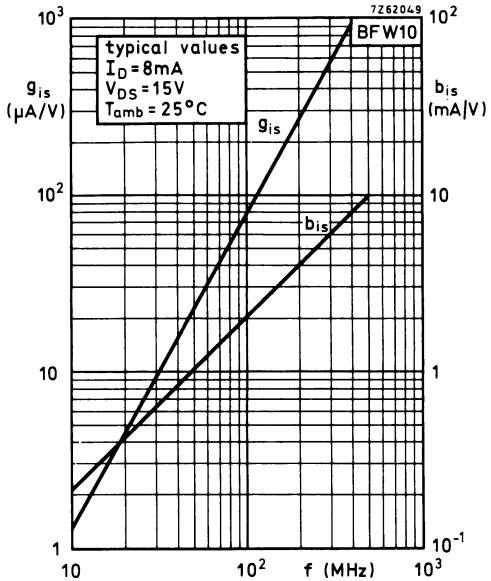

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
15
10
5
0
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

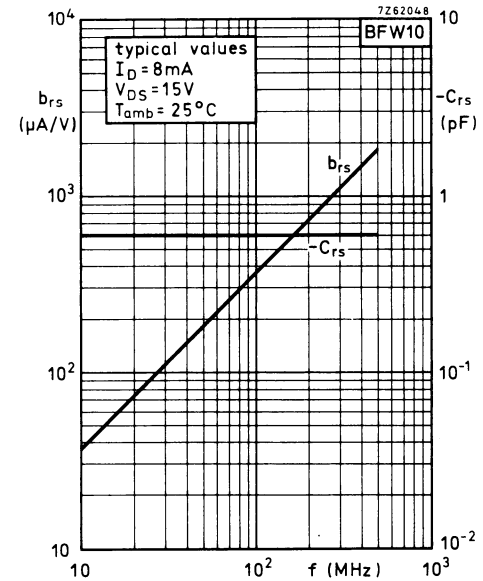

7Z62070
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

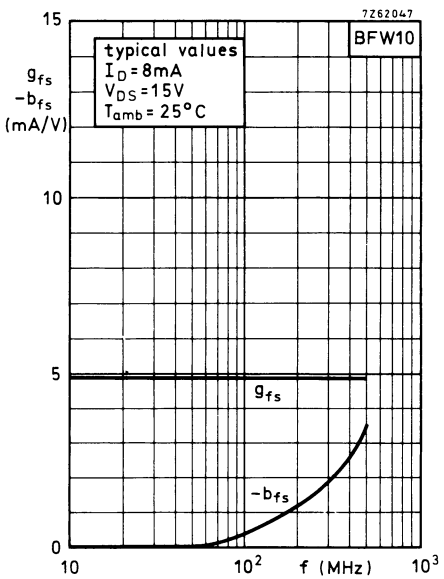

7Z62071
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

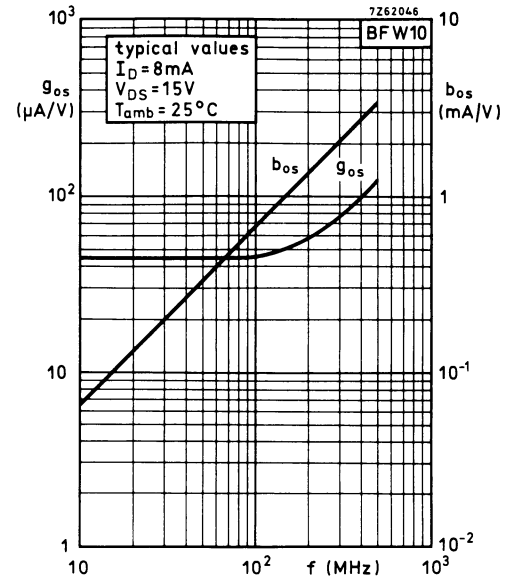

7Z62065
typical values
T_{amb} = 25 °C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
10
$-V_{GS}$ (V)

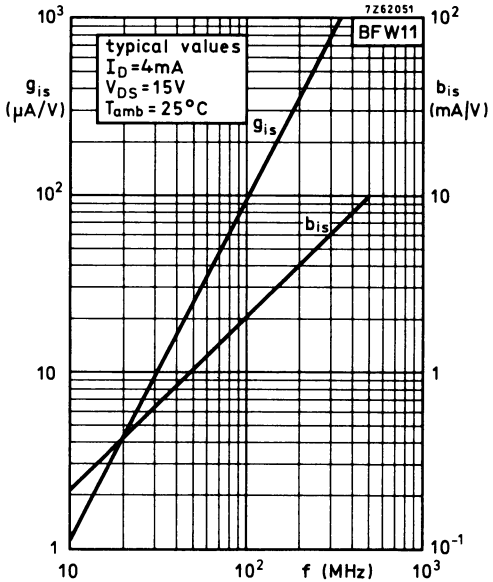

7Z62064
typical values
T_{amb} = 25 °C
C_{rs} (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
10
$-V_{GS}$ (V)

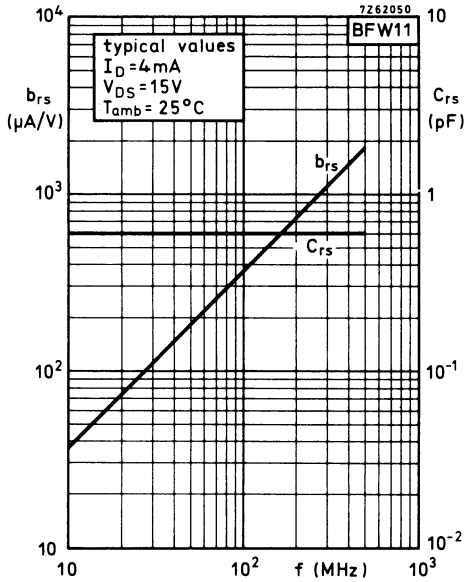

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

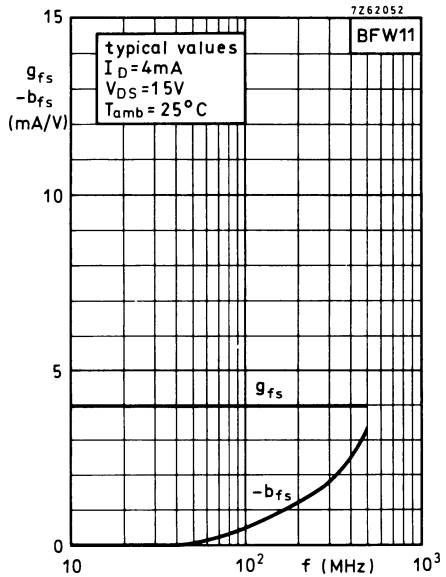

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
f (MHz)

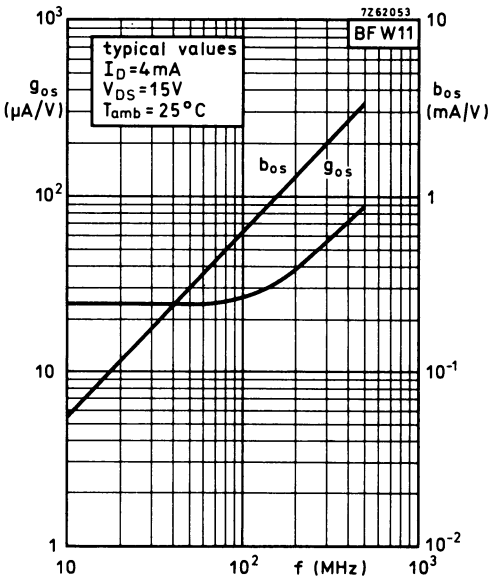

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)

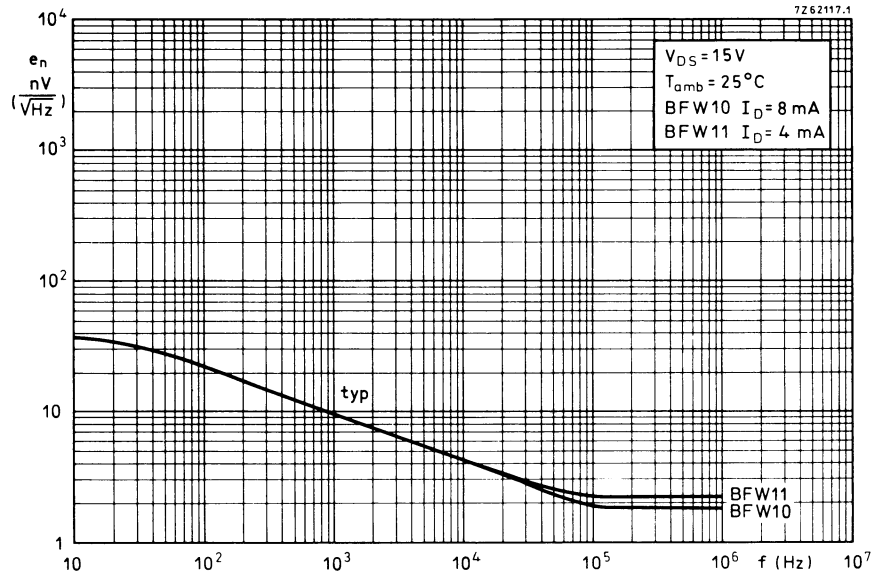

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)

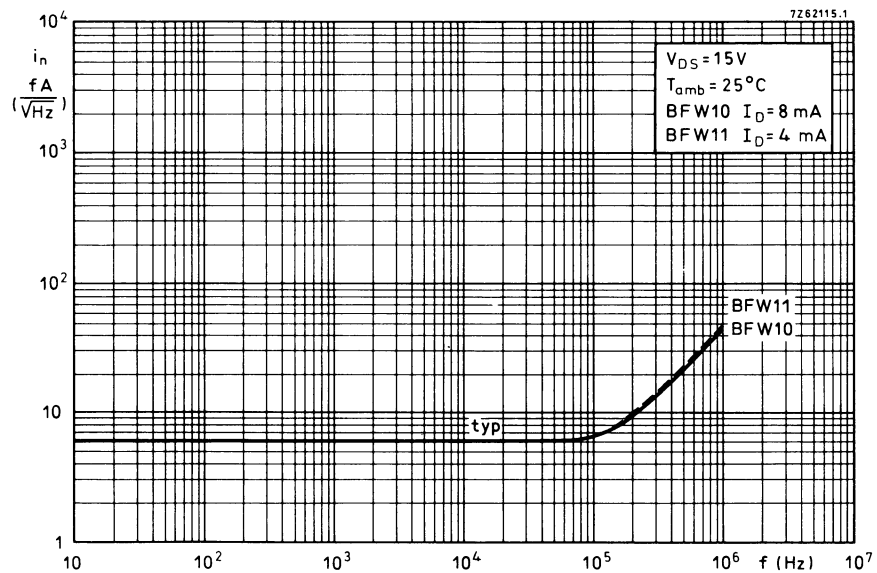

7Z62051
BFW11
typical values
I_D=4mA
V_{DS}=15V
T_{amb}=25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

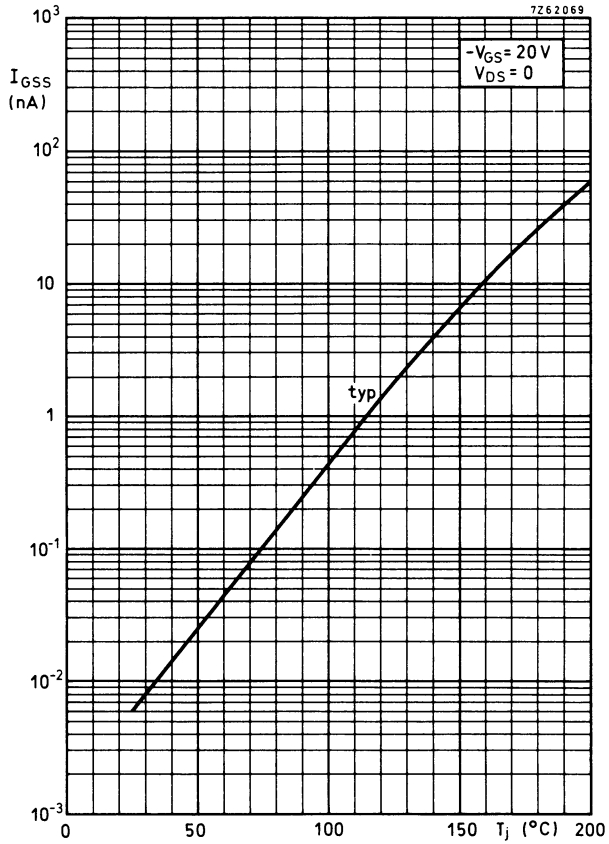

7Z62050
BFW11
typical values
I_D=4mA
V_{DS}=15V
T_{amb}=25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
f (MHz)


7Z62052
BFW11
typical values
I_D=4mA
V_{DS}=15V
T_{amb}=25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)


7Z62053
BFW11
typical values
I_D=4mA
V_{DS}=15V
T_{amb}=25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)


7Z62117.1
10^4
e_n
$\frac{nV}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62115.1
10^4
i_n
$\frac{fA}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62069
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 20 V
V_{DS} = 0
typ.
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
			BFW12	**BFW13**	
Drain current		>	1	0,2	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	5	1,5	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V, V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mS
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

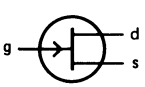
MECHANICAL DATA

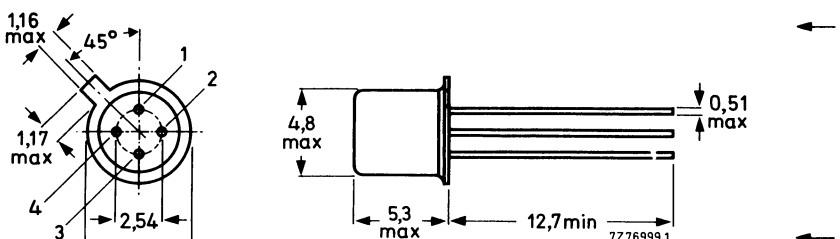
Dimensions in mm

Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case





Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150	mW
Storage temperature	T_{stg}	−65 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

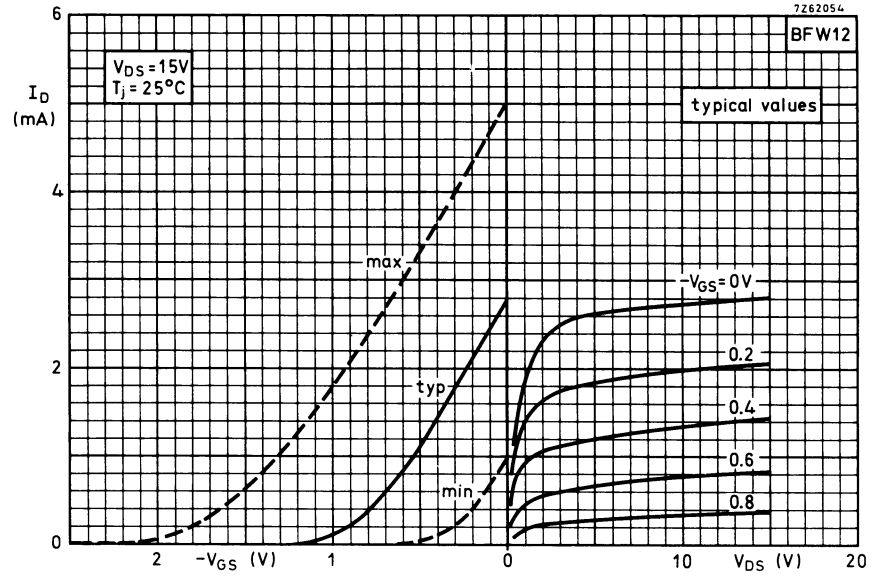
From junction to ambient	$R_{th\ j\text{-}a}$	=	**590**	**K/W**

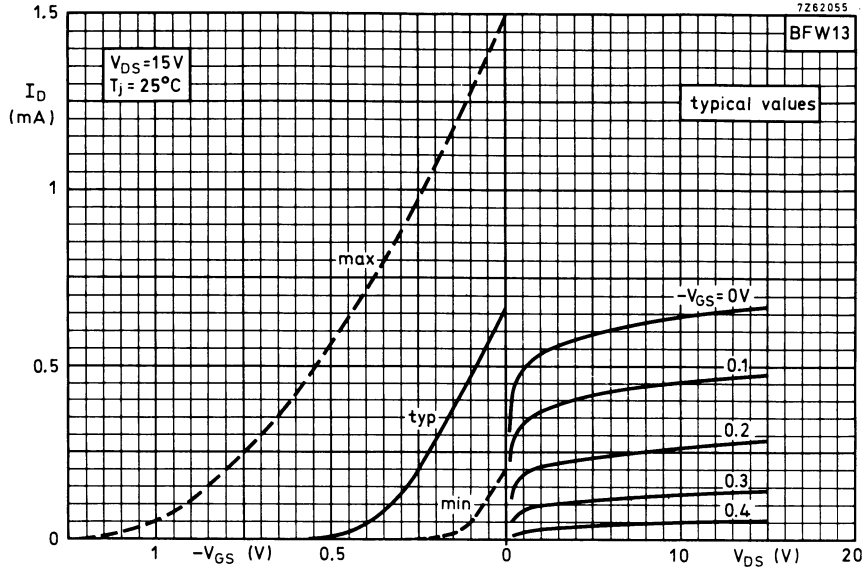
CHARACTERISTICS

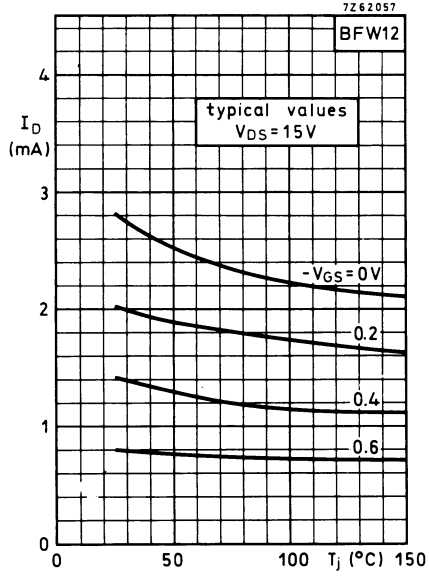
T_j = 25 °C unless otherwise specified

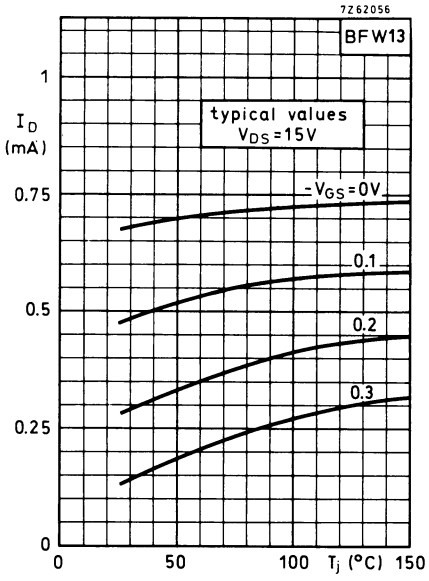
			BFW12	BFW13	
Gate cut-off currents					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	µA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 µA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	µS
V_{DS} = 15 V; I_D = 500 µA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mS
Output admittance	$\|y_{os}\|$	<	10	–	µS
V_{DS} = 15 V; I_D = 200 µA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	µS
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 µA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	µV

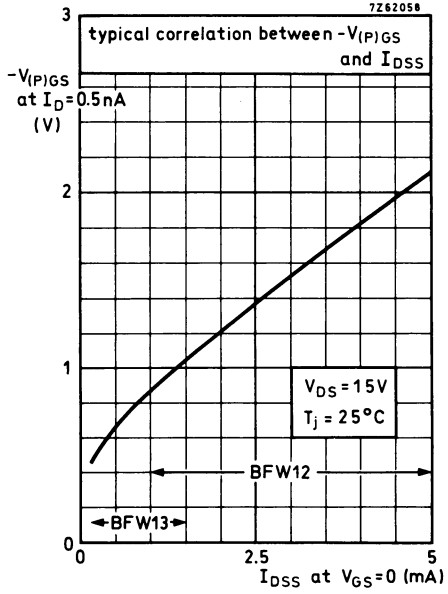
[1]) Measured under pulsed conditions.

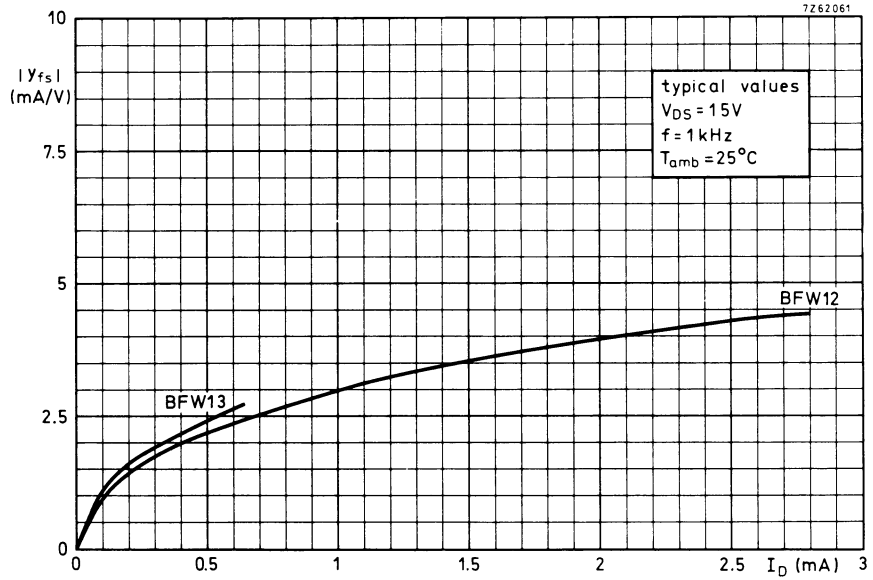

7Z62054
BFW12
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
2
$-V_{GS}$ (V)
1
0
10
V_{DS} (V)
20

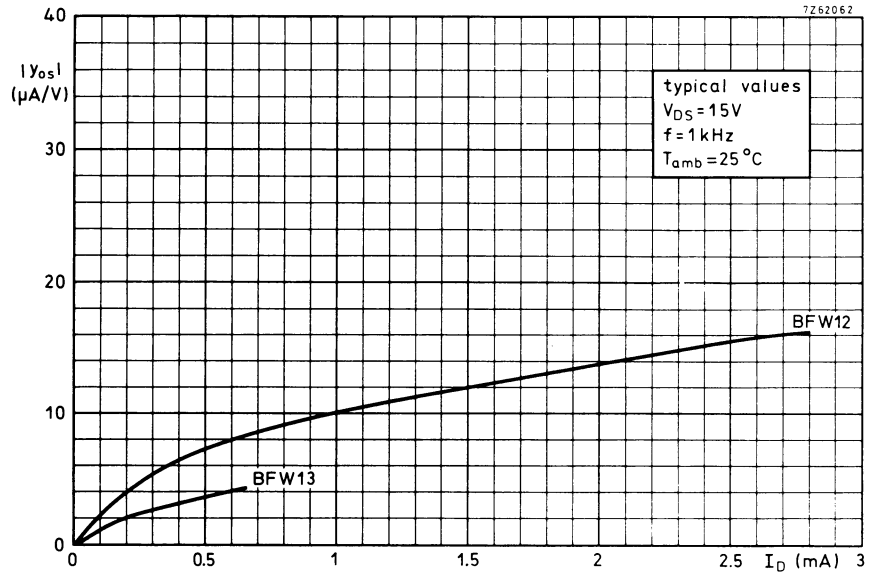

7Z62055
BFW13
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
1.5
1
0.5
0
max
typ
min
$-V_{GS}$ = 0V
0.1
0.2
0.3
0.4
1
$-V_{GS}$ (V)
0.5
0
10
V_{DS} (V)
20

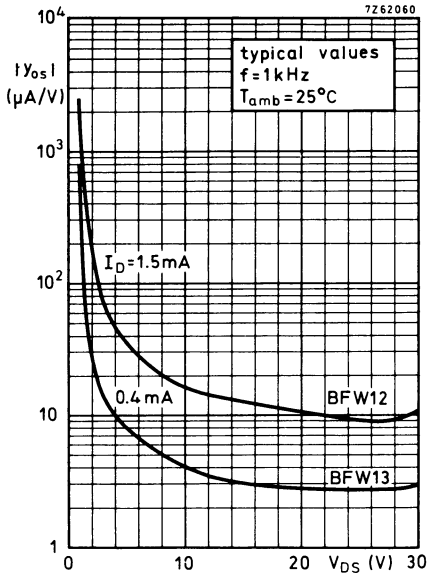

7Z62057
BFW12
typical values
V_{DS} = 15V
I_D (mA)
4
3
2
1
0
-V_{GS} = 0V
0.2
0.4
0.6
0
50
100
T_j (°C)
150

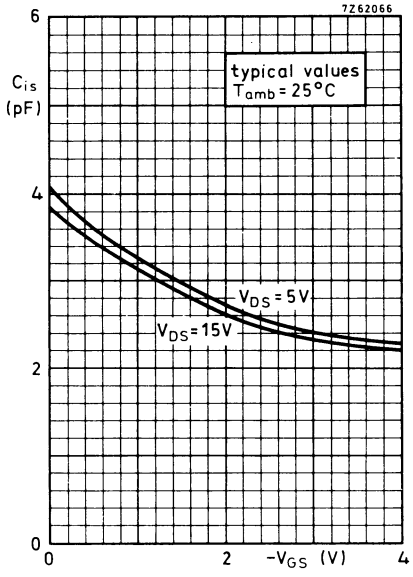

7Z62056
BFW13
typical values
V_{DS} = 15V
I_D (mA)
1
0.75
0.5
0.25
0
-V_{GS} = 0V
0.1
0.2
0.3
0
50
100
T_j (°C)
150

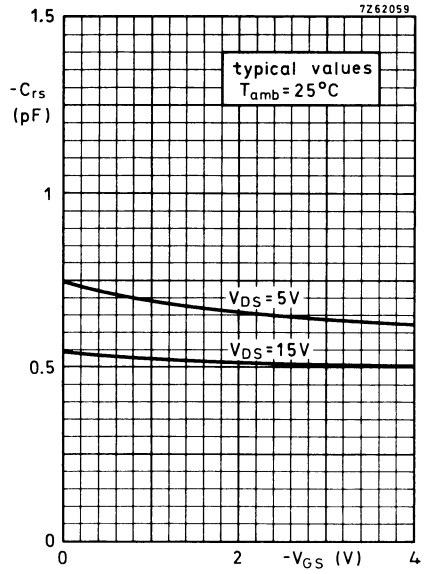

7Z62058
typical correlation between -$V_{(P)GS}$ and I_{DSS}
-$V_{(P)GS}$ at I_D = 0.5nA (V)
3
2
1
0
V_{DS} = 15V
T_j = 25°C
BFW12
BFW13
0
2.5
5
I_{DSS} at V_{GS} = 0 (mA)

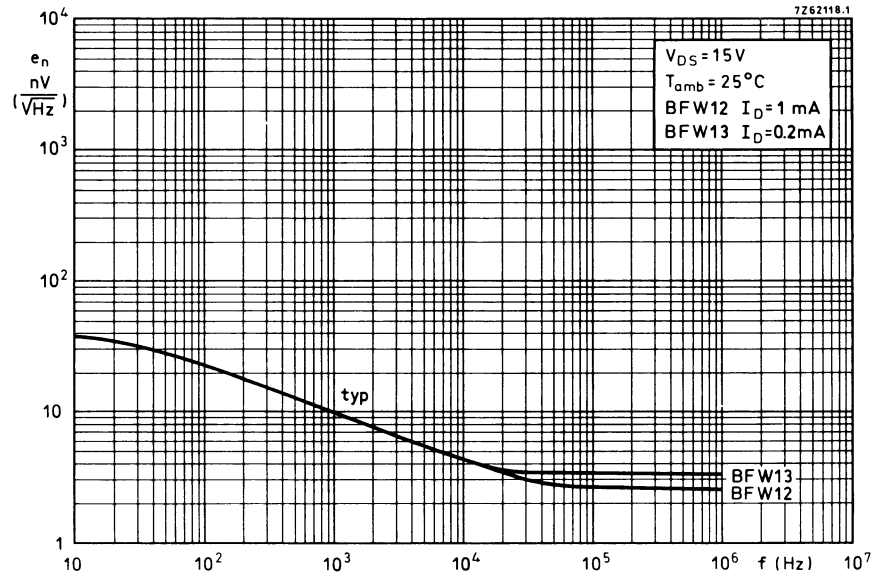

7Z62061
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

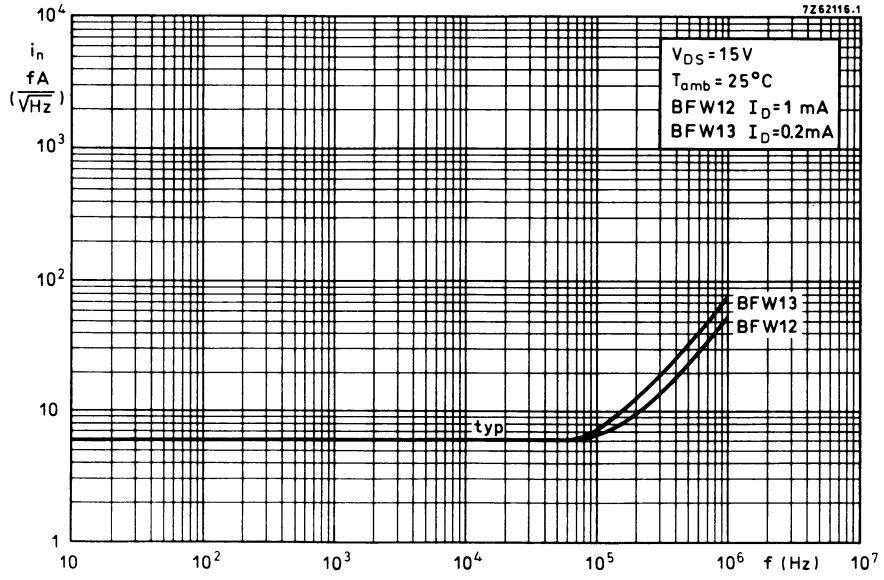

7Z62062
40
|yos|
(μA/V)
30
20
10
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

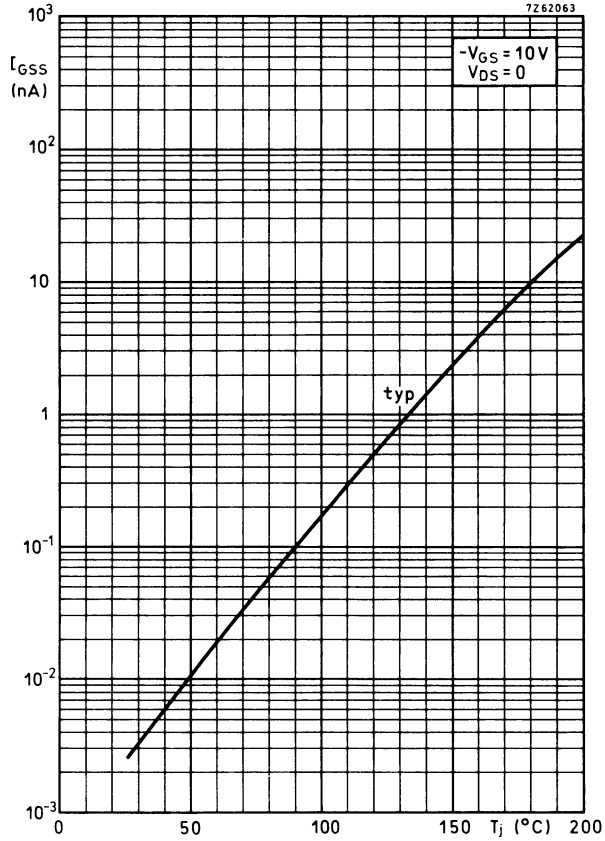

7Z62060
typical values
f = 1kHz
T_{amb} = 25°C
$|y_{os}|$ (μA/V)
10^4
10^3
10^2
10
1
I_D = 1.5mA
0.4mA
BFW12
BFW13
0
10
20
V_{DS} (V)
30


7Z62066
typical values
T_{amb} = 25°C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62059
typical values
T_{amb} = 25°C
$-C_{rs}$ (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62118.1
e_n $\frac{nV}{\sqrt{Hz}}$
10^4
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2 mA
typ
BFW13
BFW12
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62116.1
i_n $\frac{fA}{\sqrt{Hz}}$
10^4
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2 mA
BFW13
BFW12
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62063
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10 V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20 mA
Gate-source cut-off voltage I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8 V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2.0 pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 10 MHz	$\|y_{fs}\|$	>	1.6 mS

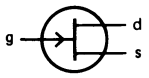
MECHANICAL DATA

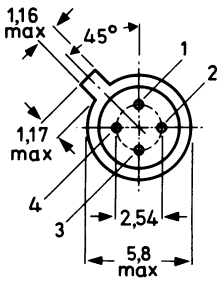
Dimensions in mm

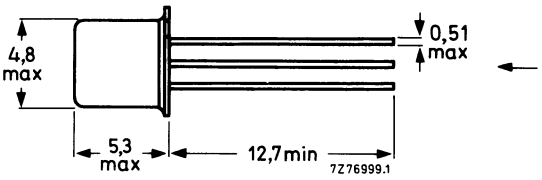
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	1.0	μA
Drain current*				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$		0.5 to 7.5	V
Gate-source cut-off voltage				
I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
y-parameters (common source)				
V_{DS} = 15 V; V_{GS} = 0				
Transfer admittance at f = 1 kHz	$\lvert y_{fs}\rvert$		2.0 to 6.5	mS
at f = 10 MHz		>	1.6	mS
Output admittance at f = 1 kHz	$\lvert y_{os}\rvert$	<	85	μS
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	2,0	pF

* Measured under pulse conditions.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

Features

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\ on}$ at zero gate voltage

QUICK REFERENCE DATA

			BSJ111	BSJ112	BSJ113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	400	400	mW
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

MECHANICAL DATA

Dimensions in mm

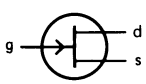
Fig.1 TO-92.

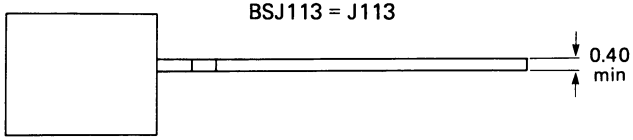
Pinning

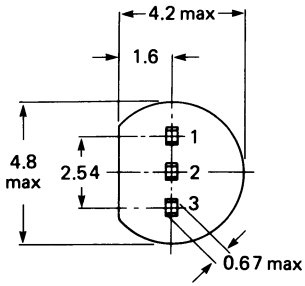
1 = Gate
2 = Source
3 = Drain

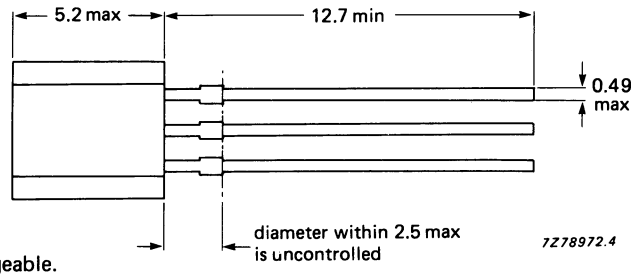
Marking code

BSJ111 = J111
BSJ112 = J112
BSJ113 = J113









Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Gate forward current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSJ111	BSJ112	BSJ113	
Gate reverse current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	1	1	1	nA
Drain cut-off current V_{DS} = 5 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	nA
Drain saturation current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{is}	typ.	6 pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz	C_{is}	typ.	22 pF
		max.	28 pF
Feedback capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rs}	typ.	3 pF
Switching times			
test conditions			
V_{DD} = 10 V; V_{GS} = 0 to V_{GSoff}			
$-V_{GS\ off}$ = 12 V; R_L = 750 Ω for BSJ111			
$-V_{GS\ off}$ = 7 V; R_L = 1550 Ω for BSJ112			
$-V_{GS\ off}$ = 5 V; R_L = 3150 Ω for BSJ113			
Rise time	t_r	typ.	6 ns
Turn-on time	t_{on}	typ.	13 ns
Fall time	t_f	typ.	15 ns
Turn-off time	t_{off}	typ.	35 ns

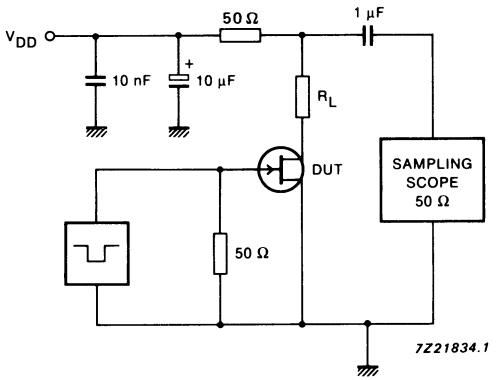


Fig.2 Switching times test circuit.

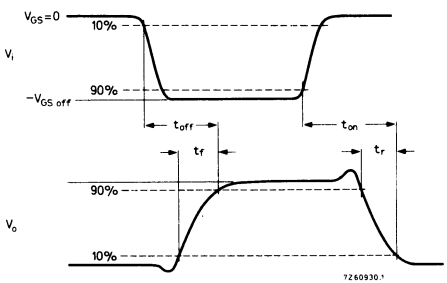


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical P-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

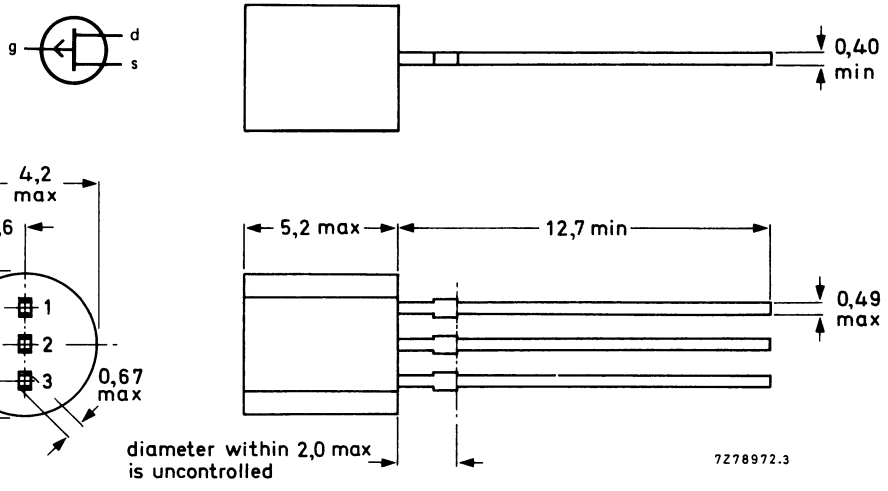
Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.		400			mW
			BSJ174	**BSJ175**	**BSJ176**	**BSJ177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:
1 = Source
2 = Gate
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSJ174	BSJ175	BSJ176	BSJ177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = 0	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	R_{DSon}	<	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)			BSJ174	BSJ175	BSJ176	BSJ177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

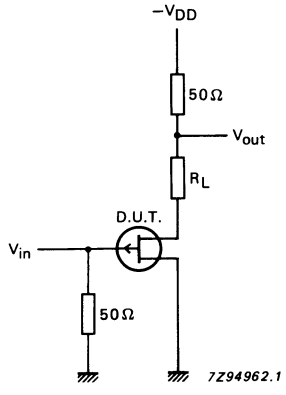


Fig. 2 Switching times test circuit.

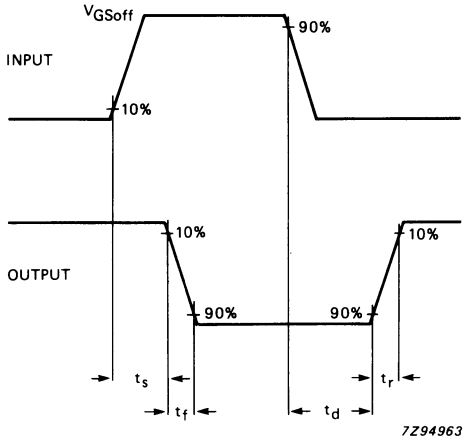


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-CHANNEL FETS

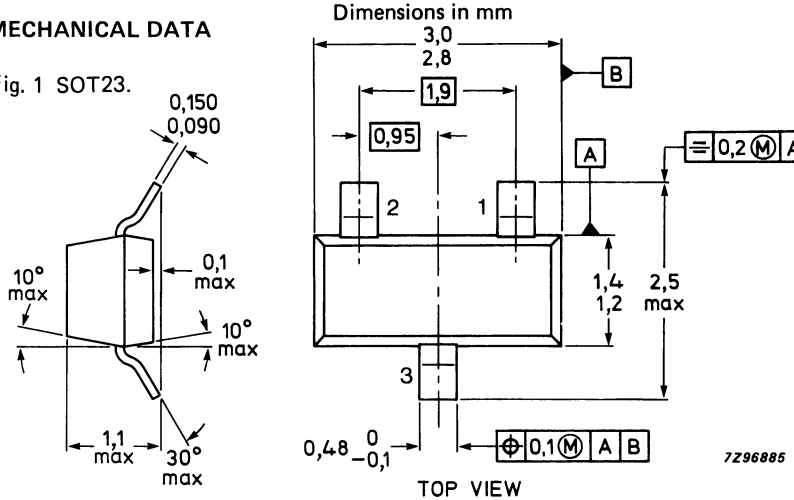
Symmetrical silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	250	250	mW
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source cut-off voltage						
V_{DS} = 15 V; I_D = 0.5 nA	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	<	5	5	5	pF
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	<	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	<	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	<	–	–	100	ns

MECHANICAL DATA

Fig. 1 SOT23.



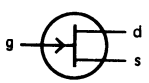
Note: Drain and source are interchangeable.

Marking code

BSR56 = M4
BSR57 = M5
BSR58 = M6

Pinning

1 = drain
2 = source
3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Forward gate current	I_{GF}	max.	50	mA
→ Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250	mW
→ Storage temperature range	T_{stg}		−65 to + 150	°C
→ Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

→ From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source cut-off current						
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	max.	1.0			nA
Drain cut-off current						
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	max.	1.0			nA
			BSR56	BSR57	BSR58	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	750	–	–	mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	500	–	mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0; T_a = 25 °C	$r_{ds\ on}$	<	25	40	60	Ω

Notes

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Switching times			BSR56	BSR57	BSR58	
V_{DD} = 10 V; V_{GS} = 0 Conditions I_D and $-V_{GSM}$	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

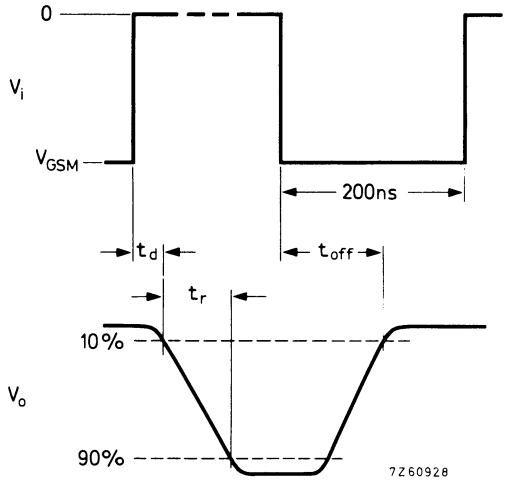


Fig. 2 Switching times waveforms.

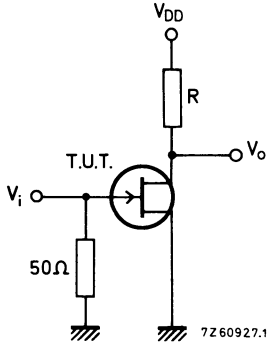


Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leqslant 1$ ns
δ = 0.02
Z_o = 50 Ω

Oscilloscope

$t_r \leqslant 0.75$ ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2.5 pF

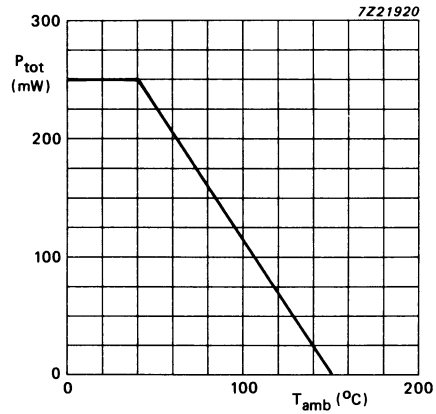


Fig.4 Power derating curve.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical n-channel junction FETs in plastic SOT23 (SMD) envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

Features

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\,on}$ at zero gate voltage

QUICK REFERENCE DATA

			BSR111	112	113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	300	300	mW
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\,off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	30	50	100	Ω

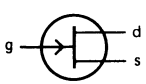
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT23.

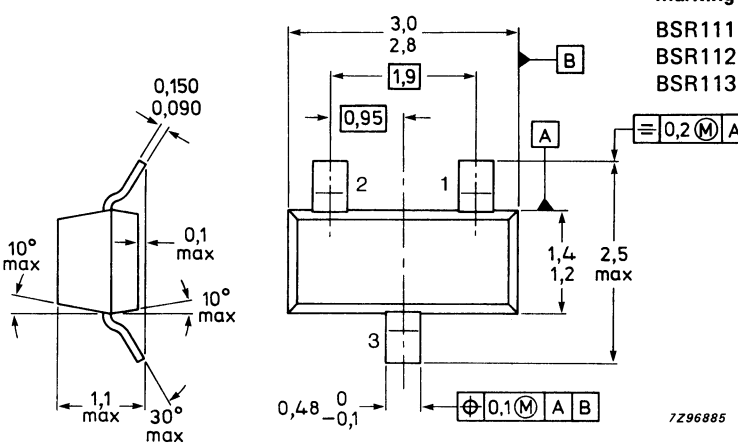
Pinning:

1 = Drain
2 = Source
3 = Gain



Marking code:

BSR111 = M41
BSR112 = M42
BSR113 = M43



TOP VIEW

Note. Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSR111	112	113	
Reverse gate current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	1	1	1	nA
Drain saturation current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min. max.	3 10	1 5	0.5 3	V V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

Note

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{iss}	typ.	6 pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	typ.	22 pF
		max.	28 pF
Feedback capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rss}	typ.	3 pF
Switching times			
test conditions:			
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\ off}$			
$-V_{GS\ off}$ = 12 V; R_L = 750 Ω for BSR111			
$-V_{GS\ off}$ = 7 V; R_L = 1550 Ω for BSR112			
$-V_{GS\ off}$ = 5 V; R_L = 3150 Ω for BSR113			
Rise time	t_r	typ.	6 ns
Turn-on time	t_{on}	typ.	13 ns
Fall time	t_f	typ.	15 ns
Turn-off time	t_{off}	typ.	35 ns

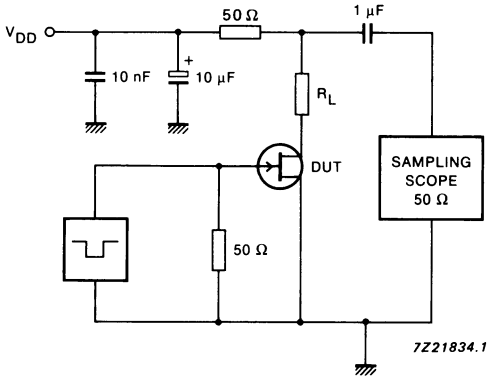


Fig.2 Switching times test circuit.

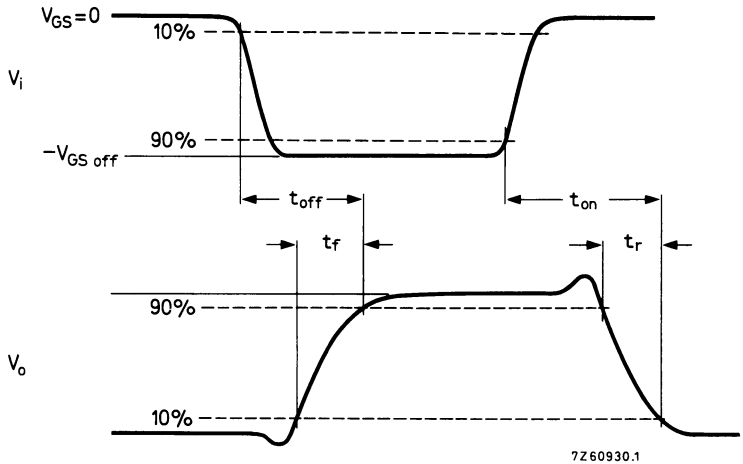


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT23 envelopes and containing a BSJ174, 175, 176 or 177 crystal.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300				mW
			BSR174	**BSR175**	**BSR176**	**BSR177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1.5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

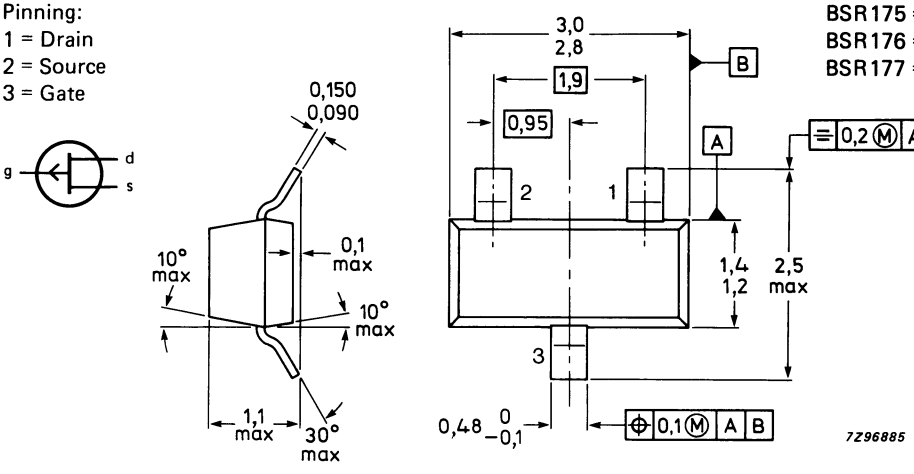
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT23.

Marking codes:
BSR174 = LO
BSR175 = LP
BSR176 = LQ
BSR177 = LR

Pinning:
1 = Drain
2 = Source
3 = Gate



TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSR174	BSR175	BSR176	BSR177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1.5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = 0	$V_{GS\,off}$	>	5	3	1	0.8	V
		<	10	6	4	2.25	V
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)			BSR174	BSR175	BSR176	BSR177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

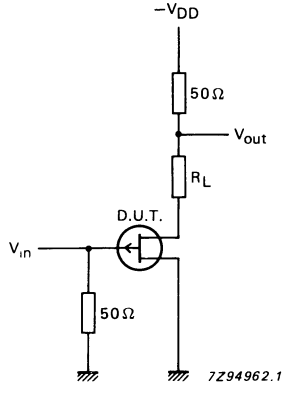


Fig. 2 Switching times test circuit.

Rise time input voltage < 1 ns

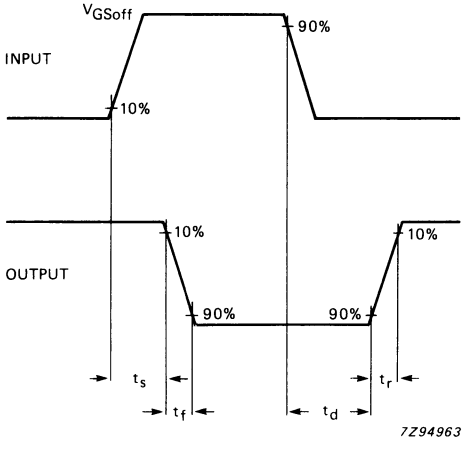


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		350		mW
			BSV78	**BSV79**	**BSV80**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

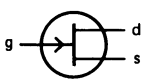
Dimensions in mm

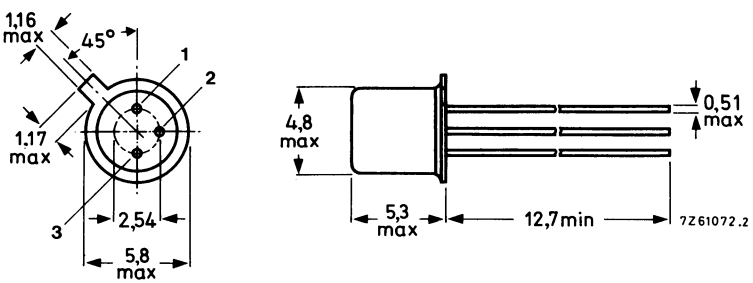
Fig. 1 TO-18.

Gate connected to case

Pinning

1 = source
2 = drain
3 = gate





Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

Products approved to CECC 50 012-011, available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Operating junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSV78	BSV79	BSV80	
Gate cut-off currents						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<		0.25		nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<		0.5		μA
Drain cut-off current						
V_{DS} = 15 V; $-V_{GS}$ = 12 V	I_{DSX}	<		0.25		nA
V_{DS} = 15 V; $-V_{GS}$ = 12 V; T_j = 150 °C	I_{DSX}	<		0.5		μA
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
I_D = 1.5 μA; V_{DS} = 15 V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	500			mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<		400		mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\,on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS}$ = 10 V; V_{DS} = 0						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF ←

Switching times (see Fig. 2)

Turn-on time when switched from

$-V_{GSoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V (**BSV78**)
$-V_{GSoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V (**BSV79**)
$-V_{GSoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V (**BSV80**)

		BSV78	BSV79	BSV80	
delay time	t_d <	5	10	10	ns
rise time	t_r <	5	8	20	ns
turn-on time	t_{on} <	10	18	30	ns

Turn-off time when switched from

I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V (**BSV78**)
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V (**BSV79**)
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V (**BSV80**)

fall time	t_f <	6	11	24	ns
storage time	t_s <	4	5	8	ns
turn-off time	t_{off} <	10	16	32	ns

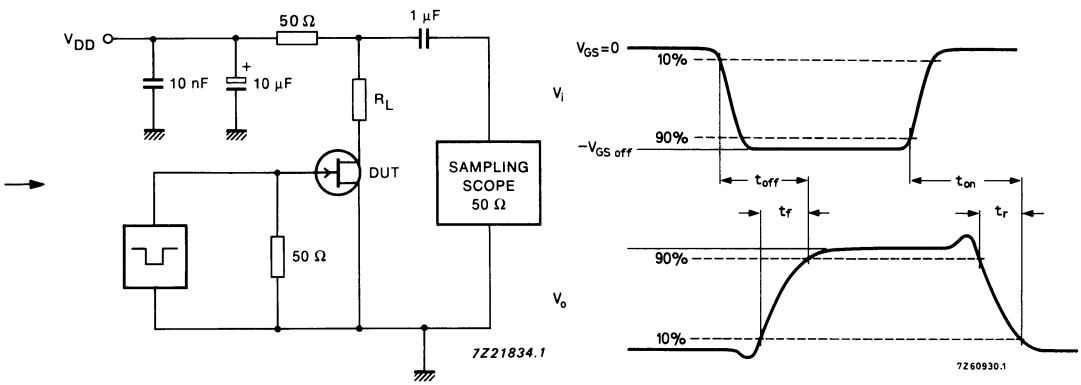


Fig. 2 Switching times test circuit and input and output waveforms.

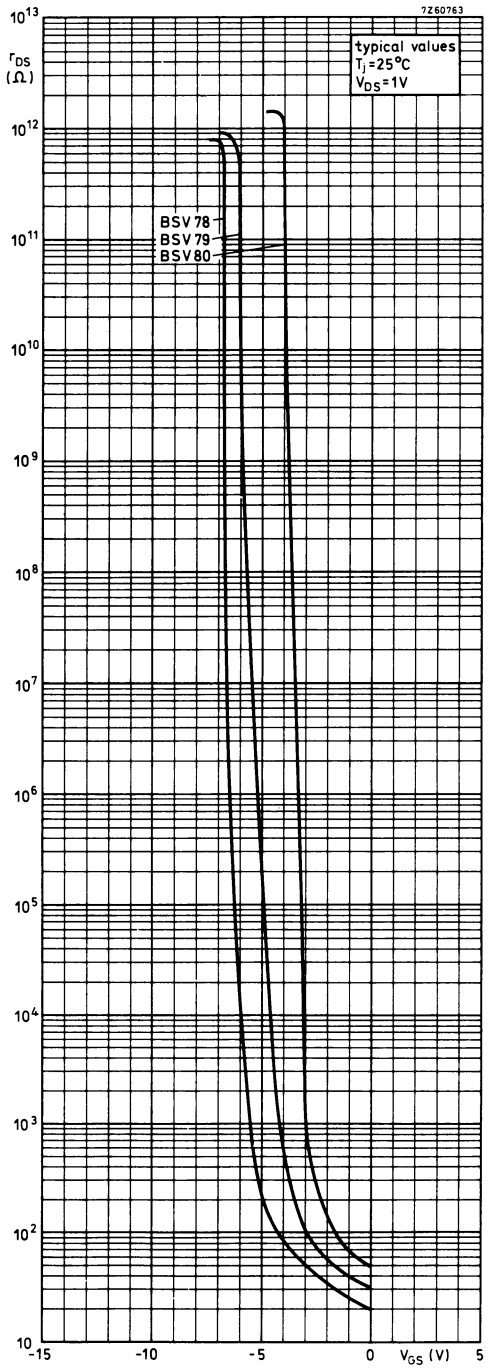
	BSV78	BSV79	BSV80	
R_L =	424	909	1885	Ω

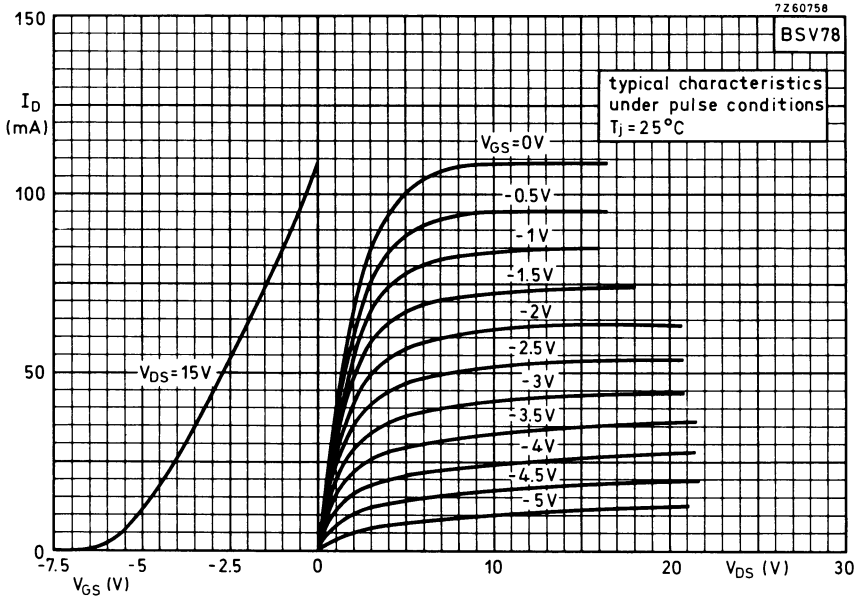
Pulse generator:

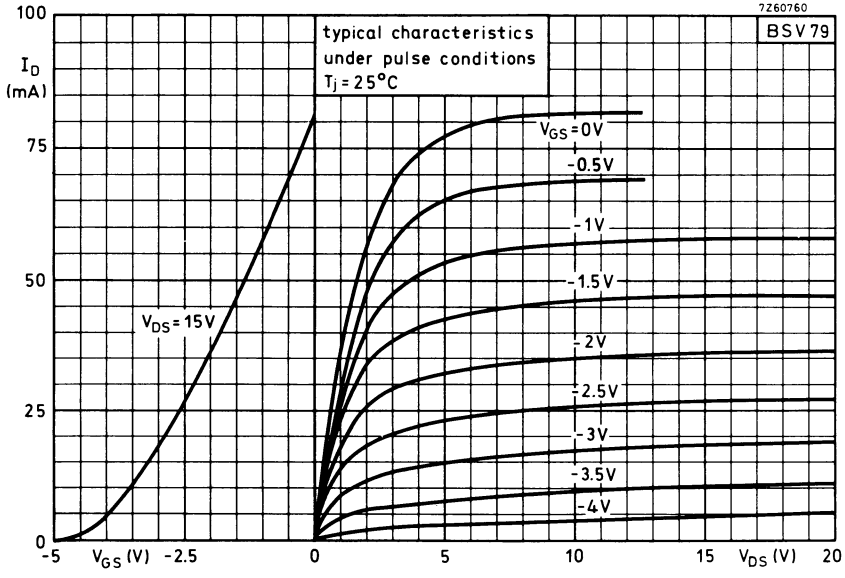
R_i = 50 Ω
t_r < 0.5 ns
t_f < 5 ns

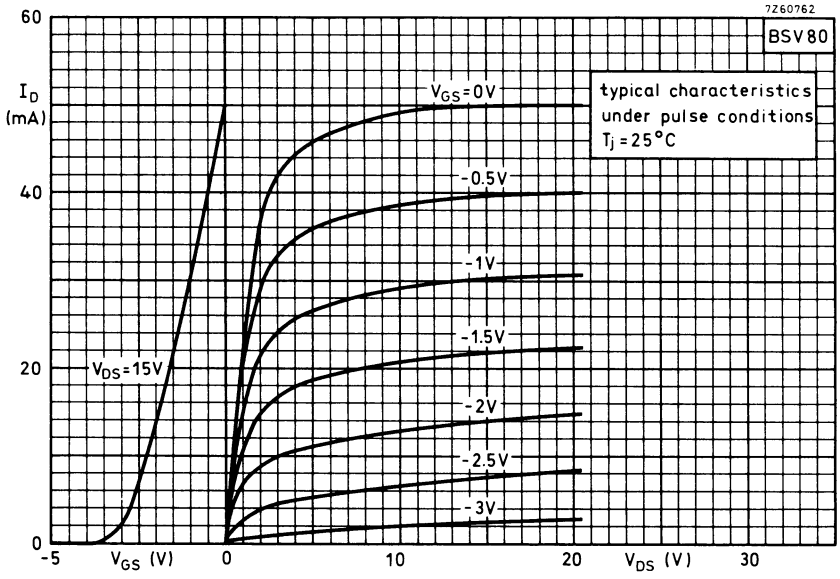
Oscilloscope:

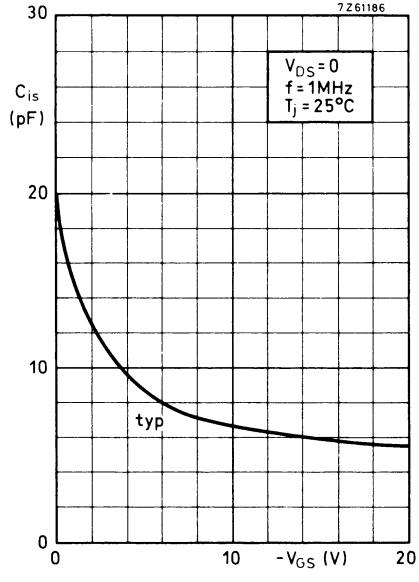
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

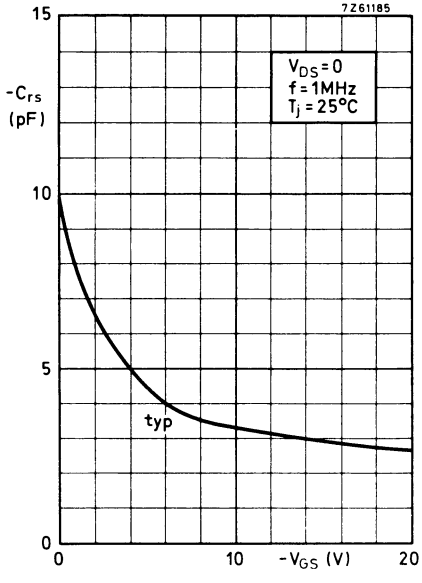

7Z60763
typical values
T_j=25°C
V_{DS}=1V
r_{DS} (Ω)
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
BSV78
BSV79
BSV80
-15
-10
-5
0
V_{GS} (V)
5

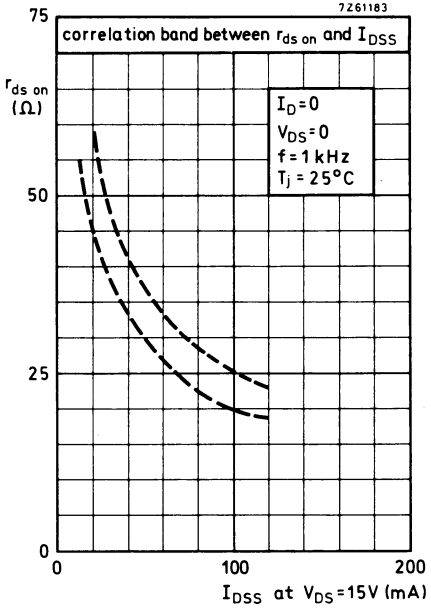

7Z60758
BSV78
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
150
100
50
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V
V_{DS}=15V
-7.5
-5
-2.5
0
10
20
30
V_{GS} (V)
V_{DS} (V)

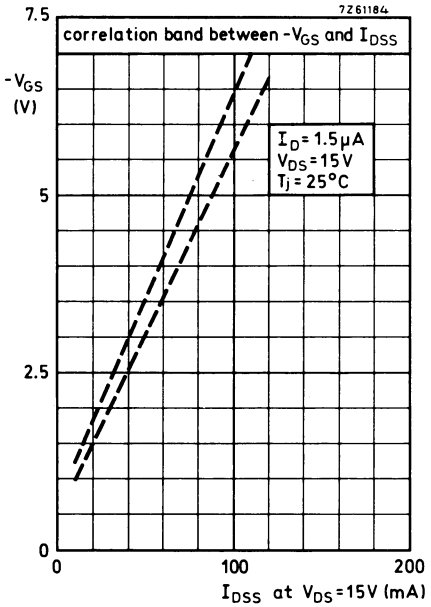

7Z60760
BSV79
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
100
75
50
25
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
V_{DS}=15V
-5
V_{GS} (V)
-2.5
0
5
10
15
20
V_{DS} (V)


7Z60762
BSV80
typical characteristics
under pulse conditions
T_j = 25 °C
I_D (mA)
V_{GS} = 0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
V_{DS} = 15V
60
40
20
0
-5
V_{GS} (V)
0
10
20
V_{DS} (V)
30


7Z61186
V_{DS} = 0
f = 1MHz
T_j = 25°C
C_{is} (pF)
30
20
10
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61185
V_{DS} = 0
f = 1MHz
T_j = 25°C
$-C_{rs}$ (pF)
15
10
5
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61183
correlation band between $r_{ds\ on}$ and I_{DSS}
$r_{ds\ on}$ (Ω)
I_D=0
V_{DS}=0
f=1 kHz
T_j=25°C
75
50
25
0
0
100
200
I_{DSS} at V_{DS}=15V (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
$-V_{GS}$ (V)
I_D=1.5μA
V_{DS}=15V
T_j=25°C
7.5
5
2.5
0
0
100
200
I_{DSS} at V_{DS}=15V (mA)

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

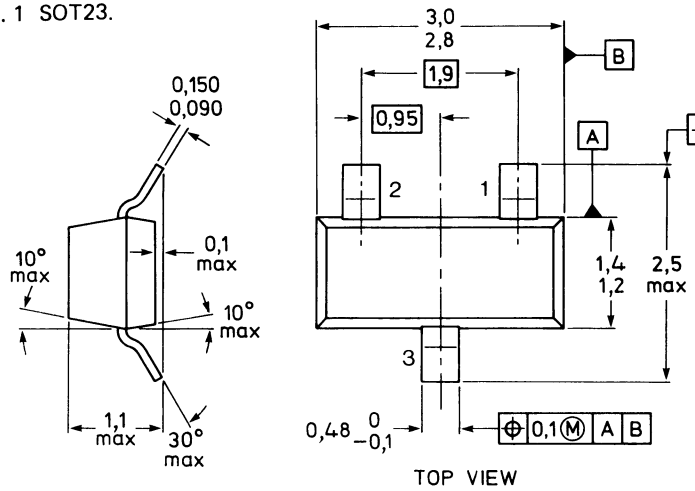
QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage		>	4	2	0,5	V
V_{DS} = 20 V; I_D = 1 nA	$-V_{(P)GS}$	<	10	5	3	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns

MECHANICAL DATA

Fig. 1 SOT23.

Dimensions in mm

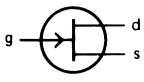


Marking code

PMBF4391 = 6J
PMBF4392 = 6K
PMBF4393 = 6G

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
→ Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250	mW
→ Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

→ From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source voltage					
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1		V
Gate-source cut-off current					
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	<	0.1		nA
V_{DS} = 0 V; $-V_{GS}$ = 20 V; T_{amb} = 150 °C	$-I_{GSS}$	<	0.2		μA

			PMBF4391	PMBF4392	PMBF4393	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
		<	150	75	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6 mA; V_{GS} = 0	V_{DSon}	<		0.4	–	V
I_D = 3 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 0; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$r_{ds\ on}$	<	30	60	100	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

			PMBF4391	PMBF4392	PMBF4393	
Drain cut-off current						
$-V_{GS}$ = 12 V } V_{DS} = 20 V	I_{DSX}	<	0.1	–	– nA	←
$-V_{GS}$ = 7 V } V_{DS} = 20 V	I_{DSX}	<	–	0.1	– nA	←
$-V_{GS}$ = 5 V } V_{DS} = 20 V	I_{DSX}	<	–	–	0.1 nA	←
$-V_{GS}$ = 12 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	0.2	–	– μA	
$-V_{GS}$ = 7 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.2	– μA	
$-V_{GS}$ = 5 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.2 μA	
y-parameters (common source)						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C						
Input capacitance	C_{is}	<	14	14	14 pF	
Feedback capacitance						
$-V_{GS}$ = 12 V	C_{rs}	<	3.5	–	– pF	←
$-V_{GS}$ = 7 V	C_{rs}	<	–	3.5	– pF	
$-V_{GS}$ = 5 V	C_{rs}	<	–	–	3.5 pF	
Switching times						
V_{DD} = 10 V; V_{GS} = 0						
Conditions I_D and $-V_{GSoff}$	I_D	=	12	6	3 mA	
	$-V_{GS\,off}$	=	12	7	5 V	
	R_L	=	750	1550	3150 Ω	←
Rise time	t_r	<	5	5	5 ns	
Turn on time	t_{on}	<	15	15	15 ns	
Fall time	t_f	<	15	20	30 ns	
Turn off time	t_{off}	<	20	35	50 ns	

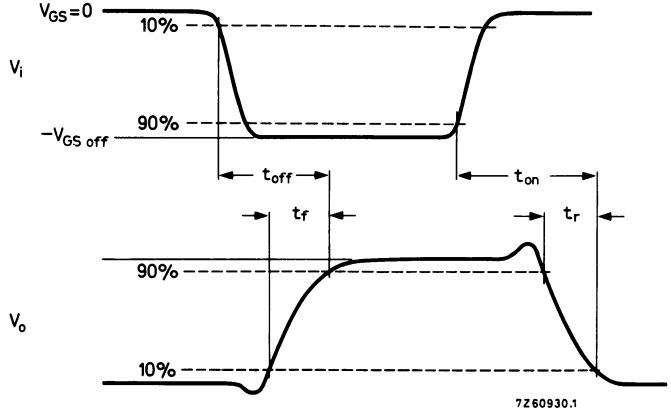
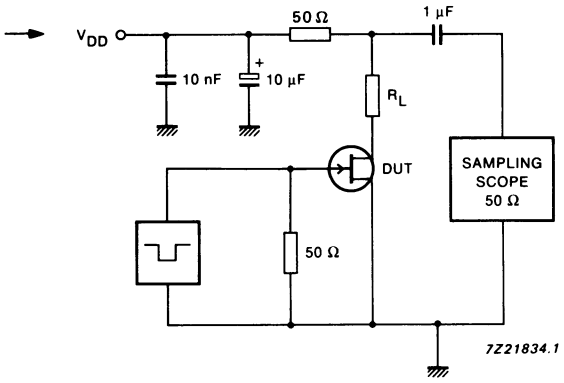


Fig.2 Switching times waveforms.



Pulse generator:

t_r < 0.5 ns
t_f < 0.5 ns
t_p = 100 μs
δ = 0.01

Oscilloscope:

R_i = 50 Ω

Fig. 3 Test circuit.

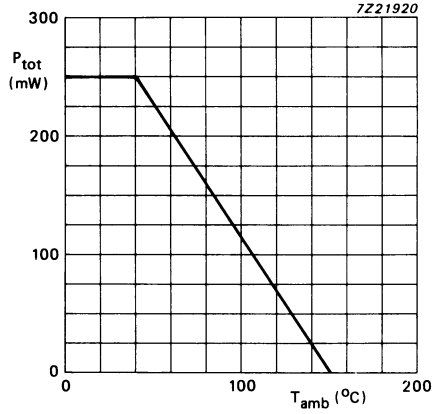


Fig.4 Power derating curve.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		300			mW
		PMBFJ174		**175**	**176**	**177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

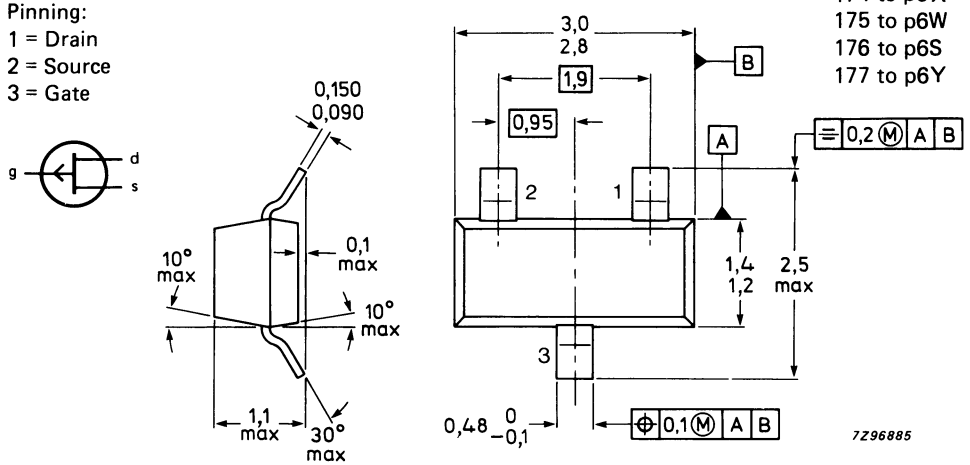
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.

Pinning:
1 = Drain
2 = Source
3 = Gate

Matching codes:
174 to p6X
175 to p6W
176 to p6S
177 to p6Y



TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air *	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = 0	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)		PMBFJ174		175	176	177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

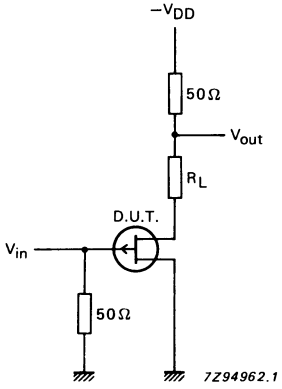


Fig. 2 Switching times test circuit.

Rise time input voltage < 1 ns

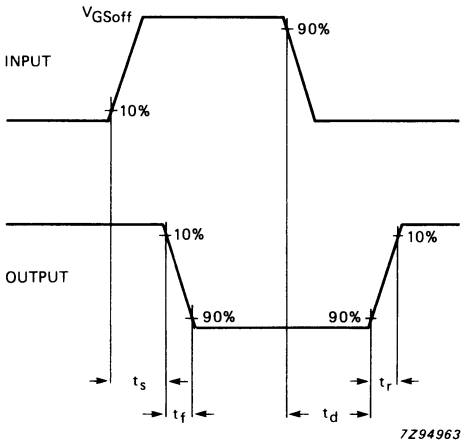


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		360	mW
			PN4391	PN4392	PN4393
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5 mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4	2	0.5 V
		max.	10	5	3 V
Drain-source on-resistance I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100 Ω

MECHANICAL DATA

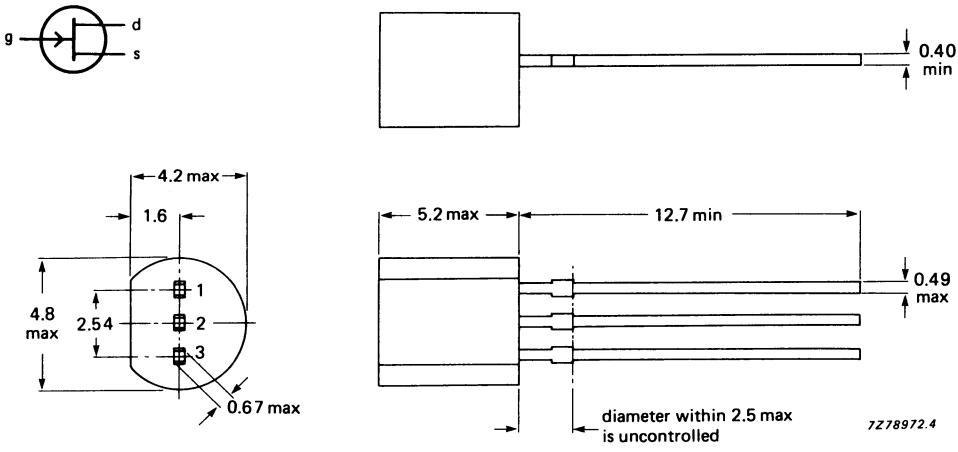
Fig.1 TO-92.

Dimensions in mm

Marking code
PN4391 = PN4391
PN4392 = PN4392
PN4393 = PN4393

Pinning

1 = Gate
2 = Source
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	350	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Reverse gate current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	1.0	1.0	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 100 °C	$-I_{GSS}$	max.	200	200	200	nA
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	max.	1.0			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	max.		1.0		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	max.			1.0	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.	200			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.		200		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.			200	nA
Drain saturation current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
		max.	150	100	60	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage						
V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4.0	2.0	0.5	V
		max.	10	5.0	3.0	V
Drain-source on-resistance						
I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω
Drain-source on-voltage						
V_{GS} = 0; I_D = 12 mA	$V_{DS\,on}$	max.	0.4			V
V_{GS} = 0; I_D = 6 mA	$V_{DS\,on}$	max.		0.4		V
V_{GS} = 0; I_D = 3 mA	$V_{DS\,on}$	max.			0.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Drain-source on-resistance						
V_{DS} = 0; V_{GS} = 0; f = 1 kHz; T_a = 25 °C	$R_{DS\,on}$	max.	30	60	100	Ω
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	max.	16	16	16	pF
Feedback capacitance						
V_{DS} = 0; $-V_{GS}$ = 12 V, f = 1 MHz	C_{rss}	max.	5			pF
V_{DS} = 0; $-V_{GS}$ = 7 V, f = 1 MHz	C_{rss}	max.		5		pF
V_{DS} = 0; $-V_{GS}$ = 5 V, f = 1 MHz	C_{rss}	max.			5	pF
Switching times						
test conditions						
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\,off}$	I_D	=	12	6.0	3.0	mA
	$-V_{GS\,off}$	=	12	7.0	5.0	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	max.	5	5	5	ns
Turn-on time	t_{on}	max.	15	15	15	ns
Fall time	t_f	max.	15	20	30	ns
Turn-off time	t_{off}	max.	20	35	50	ns

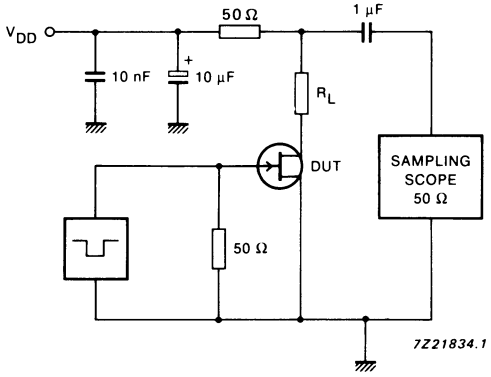


Fig.2 Switching times test circuit.

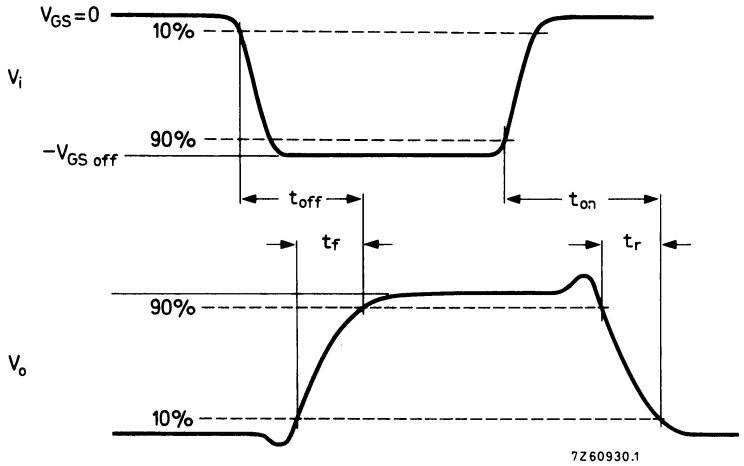


Fig.3 Input and output waveforms.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Drain current			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10 mA
Transfer admittance (common source)			
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$		3,0 to 6,5 mS
V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	$\|y_{fs}\|$	>	3,0 mS

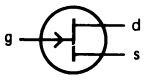
MECHANICAL DATA

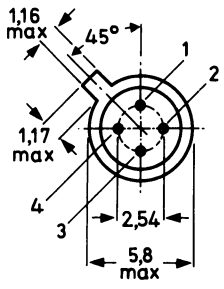
Dimensions in mm

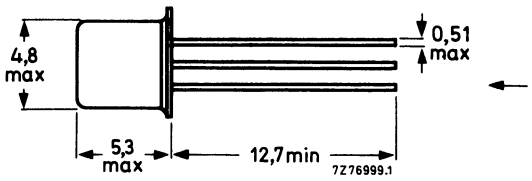
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50	V
Drain-gate voltage	V_{DG}	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS with source connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 30 V; V_{DS} = 0	$-I_{GSS}$	<	0,1	nA
$-V_{GS}$ = 30 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,1	μA
Drain current *				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10	mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	50	V
Gate-source voltage				
V_{DS} = 15 V; I_D = 200 μA	$-V_{GS}$		1 to 4	V
Gate-source cut-off voltage				
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	6	V
Small-signal common source characteristics				
V_{DS} = 15 V; V_{GS} = 0				
Transfer admittance *				
f = 1 kHz	$\lvert y_{fs} \rvert$		3,0 to 6,5	mS
f = 100 MHz	$\lvert y_{fs} \rvert$	>	3,0	mS
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	20	μS
→ Input capacitance at f = 1 MHz	C_{iss}	<	6	pF
→ Feedback capacitance at f = 1 MHz	C_{rss}	<	3	pF
Noise figure				
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 MΩ				
f = 10 Hz; B = 5 Hz	F	<	5	dB
Equivalent input noise voltage				
V_{DS} = 15 V; V_{GS} = 0				
f = 10 Hz; B = 5 Hz	V_n	<	200	$nV/\sqrt{Hz}$

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

QUICK REFERENCE DATA

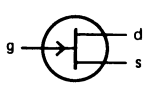
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20	mA
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rss}	<	2	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	mS
Noise figure at f = 100 MHz V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5	dB

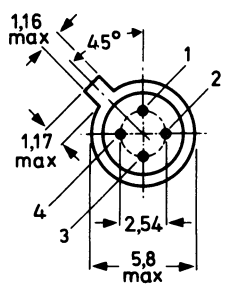
MECHANICAL DATA

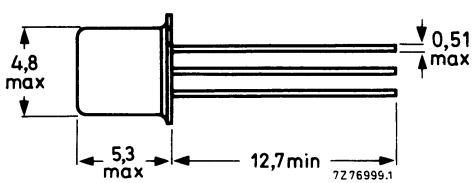
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage	V_{DG}	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		−65 to + 200 °C
Junction temperature	T_j	max.	200 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590 K/W

CHARACTERISTICS with source and shield connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0,5 nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,5 μA
Drain current *			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20 mA
Gate-source breakdown voltage			
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30 V
Gate-source voltage			
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$		1,0 to 7,5 V
Gate-source cut-off voltage			
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	8 V
Small-signal common source characteristics			
V_{DS} = 15 V; V_{GS} = 0			
Transfer admittance *			
f = 1 kHz	$\lvert y_{fs} \rvert$		3,5 to 6,5 mS
f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2 mS
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	35 μS
→ Input capacitance at f = 1 MHz	C_{iss}	<	6 pF
→ Feedback capacitance at f = 1 MHz	C_{rss}	<	2 pF
Real part of input conductance at f = 200 MHz	$Re(y_{is})$	<	0,8 mS
Real part of output conductance at f = 200 MHz	$Re(y_{os})$	<	0,2 mS
Noise figure at f = 100 MHz			
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5 dB

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

QUICK REFERENCE DATA

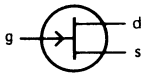
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Feedback capacitance at f = 1 MHz V_{DS} = 0; V_{GS} = 7 V	C_{rs}	<	1,5	pF
Drain-source resistance (on) at f = 1 kHz V_{GS} = 0; I_D = 0	R_{DSon}	<	220	Ω

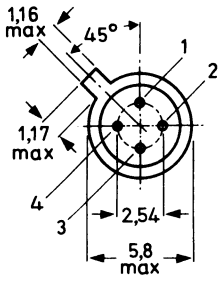
MECHANICAL DATA

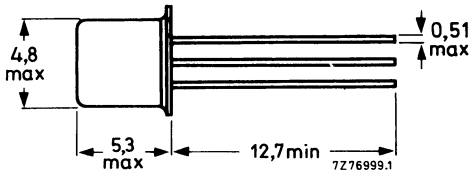
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−55 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	**590**	**K/W**

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	nA
Drain current				
V_{DG} = 20 V; I_S = 0	I_{DGO}	<	0.1	nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<	0.2	μA
Drain current [1])				
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source breakdown voltage				
$-I_G$ = 1.0 μA; V_{DS} = 0	$-V_{(BR)GS}$	>	30	V
Gate-source voltage				
I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Drain-source voltage				
I_D = 1.0 mA; V_{GS} = 0	V_{DS}	<	0.25	V
Drain cut-off current				
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V	I_D	<	1.0	nA
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V; T_{amb} = 150 °C	I_D	<	2.0	μA
Drain-source resistance (on) at f = 1 kHz				
V_{GS} = 0; I_D = 0	R_{DSon}	<	220	Ω
Input capacitance at f = 1 MHz				
V_{DS} = 20 V; V_{GS} = 0	C_{iss}	<	6	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 0; V_{GS} = 7 V	C_{rss}	<	1.5	pF
Switching times				
V_{DD} = 1.5 V; $I_{D\,on}$ = 1.0 mA				
$V_{GS\,on}$ = 0; $-V_{GS\,off}$ = 6 V				
delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

CHARACTERISTICS (continued)

Switching times

V_{DD} = 1.5 V; $I_{D\,on}$ = 1.0 mA

$V_{GS\,on}$ = 0; $-V_{GS\,off}$ = 6 V

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

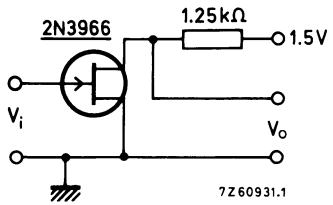


Fig. 2 Test circuit

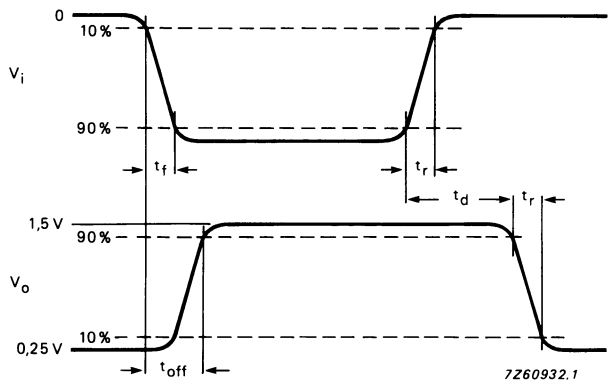


Fig. 3 Waveforms

Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 µs
δ < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage		$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C		P_{tot}	max		1,8		W
				2N4091	**2N4092**	**2N4093**	
Drain current							
V_{DS} = 20 V; V_{GS} = 0		I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage			>	5,0	2,0	1,0	V
I_D = 1 nA; V_{DS} = 20 V		$-V_{(P)GS}$	<	10	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz							
I_D = 0; V_{GS} = 0		$R_{DS\ on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz							
V_{DS} = 0; $-V_{GS}$ = 20 V		C_{rs}	<		5,0		pF
Turn-off time							
V_{DD} = 3,0 V; V_{GS} = 0							
I_D = 6,6 mA; $-V_{GSM}$ = 12 V	**2N4091**	t_{off}	<		40		ns
I_D = 4,0 mA; $-V_{GSM}$ = 8 V	**2N4092**	t_{off}	<		60		ns
I_D = 2,5 mA; $-V_{GSM}$ = 6 V	**2N4093**	t_{off}	<		80		ns

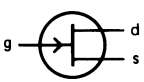
MECHANICAL DATA

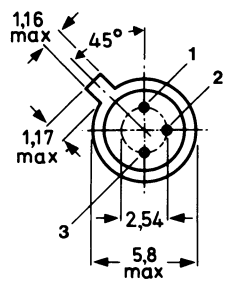
Dimensions in mm

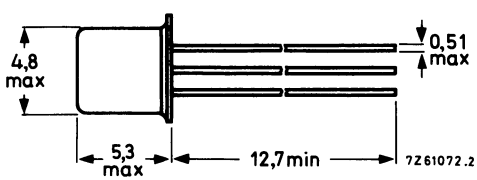
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Current				
Forward gate current (DC)	I_G	max.	10	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.8	W
Storage temperature	T_{stg}	−55 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

→ From junction to case in free air	$R_{th\ j\text{-}c}$	=	**100**	**K/W**

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain currents

			2N4091	2N4092	2N4093	
V_{DG} = 20 V; I_S = 0	I_{DGO}	<	0.2			nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<	0.4			μA
Source current						
V_{SG} = 20 V; I_D = 0	I_{SGO}	<	0.2			nA
Drain cut-off current			2N4091	2N4092	2N4093	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX}	<	0.4	–	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.4	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.4	μA
Gate-source breakdown voltage						
$-I_G$ = 1.0 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Drain current [1])						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V
Drain-source voltages (on)						
I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V
Drain- source resistance (on)						
I_D = 1.0 mA; V_{GS} = 0	R_{DSon}	<	30	50	80	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω

[1]) Measured under pulsed conditions: $t_p \leq 300$ μs; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

Input capacitance

V_{DS} = 20 V ; V_{GS} = 0 C_{is} < 16 pF

Feedback capacitance

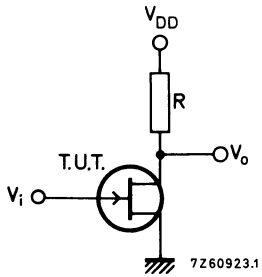
V_{DS} = 0 ; $-V_{GS}$ = 20 V C_{rs} < 5 pF

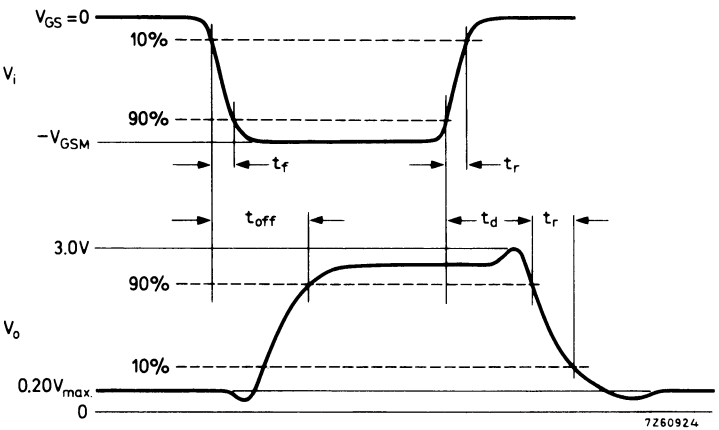
Switching times

V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:





$$R = \frac{2,8}{I_D}$$

Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1,8		W
			2N4391	**2N4392**	**2N4393**	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage		>	4,0	2,0	0,5	V
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz						
V_{DS} = 0; $-V_{GS}$ = 12 V **2N4391**	C_{rs}	<	3,5	3,5	3,5	pF
V_{DS} = 0; $-V_{GS}$ = 7 V **2N4392**						
V_{DS} = 0; $-V_{GS}$ = 5 V **2N4393**						
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSoff}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSoff}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSoff}$ = 5 V	t_{off}	<	–	–	50	ns

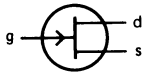
MECHANICAL DATA

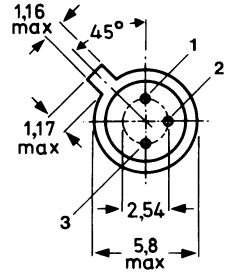
Dimensions in mm

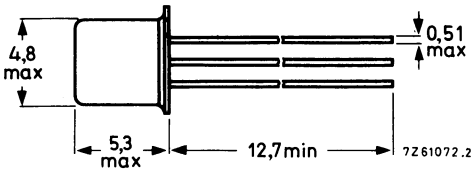
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.8	W
Storage temperature	T_{stg}	−65 to	200	°C
Junction temperature	T_j	max.	200	°C
From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off current

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$ <	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$ <	0.2	µA

Drain cut-off current

		2N4391	2N4392	2N4393	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX} <	0.1	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 7 V	I_{DSX} <	–	0.1	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 5 V	I_{DSX} <	–	–	0.1	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX} <	0.2	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 7 V; T_{amb} = 150 °C	I_{DSX} <	–	0.2	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 5 V; T_{amb} = 150 °C	I_{DSX} <	–	–	0.2	µA

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain currents (note 1)						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

Note

1. measured under pulsed conditions: t_p = 100 µs; δ = 0.01

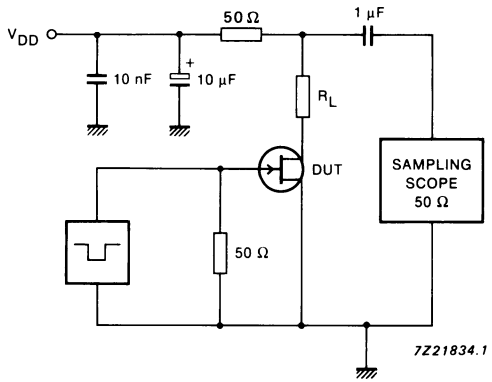
CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

Switching times

V_{DD} = 10 V; V_{GS} = 0

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSoff}$	=	12	7	5	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:

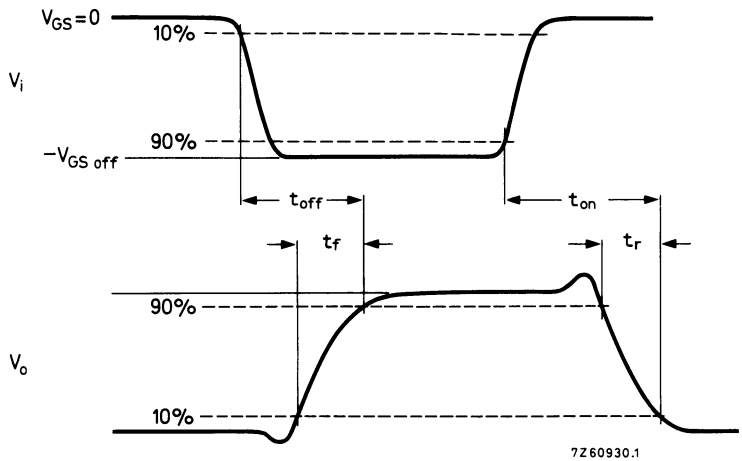


Pulse generator:

t_r	< 0.5	ns
t_f	< 0.5	ns
t_p	= 100	µs
δ	= 0.01	

Oscilloscope:

R_i = 50 Ω



N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	**2N4856 to 2N4858**	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
				2N4856 2N4859	**2N4857 2N4860**	**2N4858 2N4861**	
Drain current							
V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage			>	4	2	0,8	V
I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz							
I_D = 0; V_{GS} = 0		$R_{DS\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz							
V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time							
V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

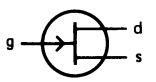
MECHANICAL DATA

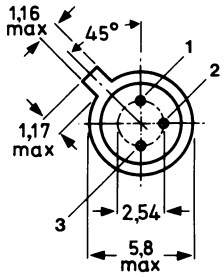
Dimensions in mm

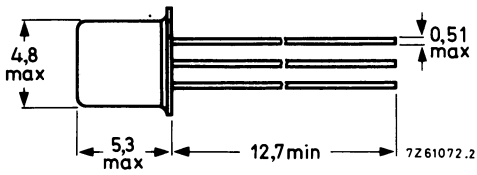
Fig. 1 TO-18

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Gate current (d.c.)	I_G	max.	50		mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	360		mW
Storage temperature	T_{stg}		−65 to +200		^oC
Junction temperature	T_j	max.	200		^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	**490**	**K/W**

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	μA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	μA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	μA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage					
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	25	40	60	Ω

[1]) measured under pulsed conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz

Input capacitance	C_{is}	<	18	pF
Feedback capacitance	C_{rs}	<	8	pF

Switching times (see Figs 2 and 3)
V_{DD} = 10 V; V_{GS} = 0

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	=	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

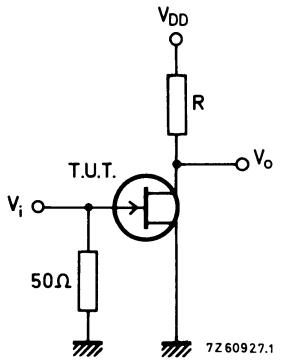


Fig. 2 Switching times test circuit.

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
R =	464	953	1910	Ω

Pulse generator:
$t_r \leqslant$ 1 ns
$t_f \leqslant$ 1 ns
δ = 0,02
Z_o = 50 Ω

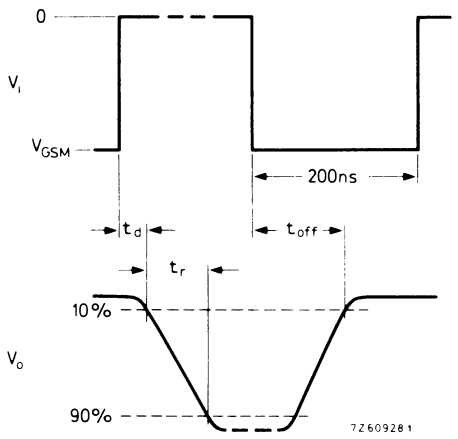


Fig. 3 Input and output waveforms.

Oscilloscope:
$t_r \leqslant$ 0,75 ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

DEVICE DATA
MOS-FETs
single gate

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		10 to 40 mA
Transfer admittance I_D = 5 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	6 mS
Feedback capacitance I_D = 5 mA; V_{DS} = 15 V; f = 1 MHz	C_{rs}	<	0,7 pF
Noise figure at f = 200 MHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C G_S = 1 mS; $B_S = B_{Sopt}$	F	<	5 dB
Equivalent noise voltage at f = 1 kHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C	$V_n\sqrt{B}$	typ.	100 $nV\sqrt{Hz}$

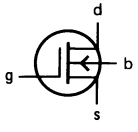
MECHANICAL DATA

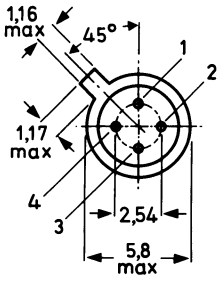
Dimensions in mm

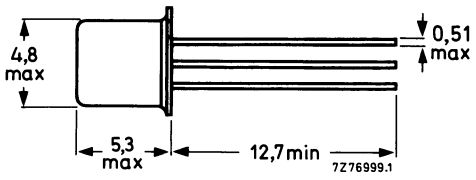
Fig. 1 TO-72.

Pinning

1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 −15	V V
Drain current (d.c.)	I_D	max.	20	mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to +	125	°C
Junction temperature	T_j	max.	125	°C

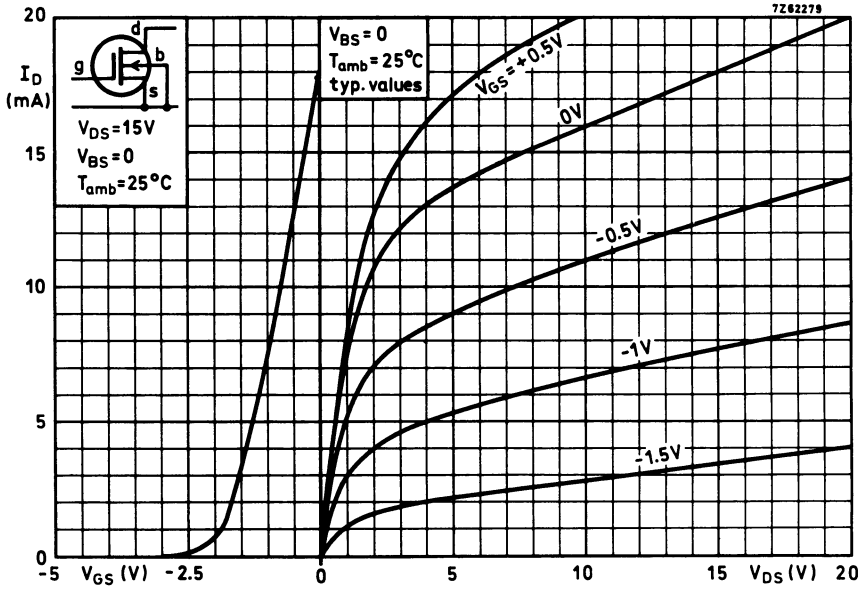
THERMAL RESISTANCE

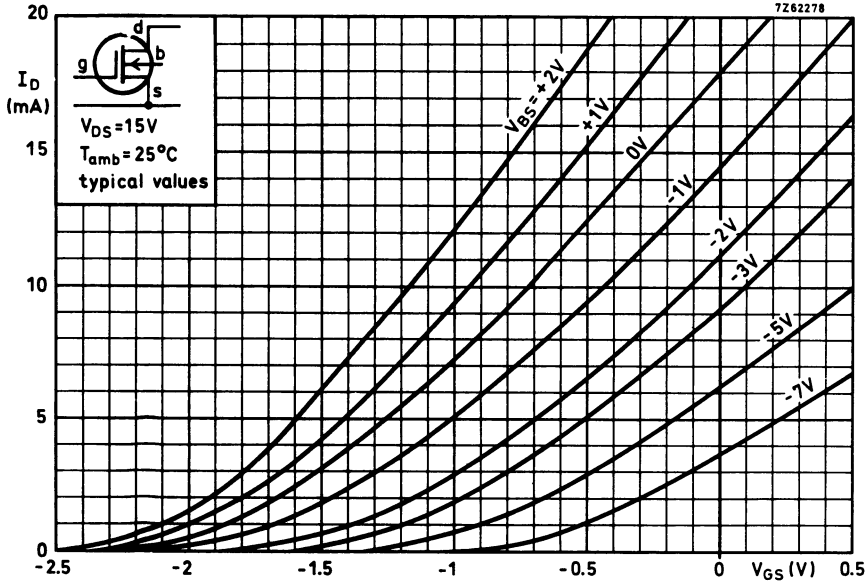
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

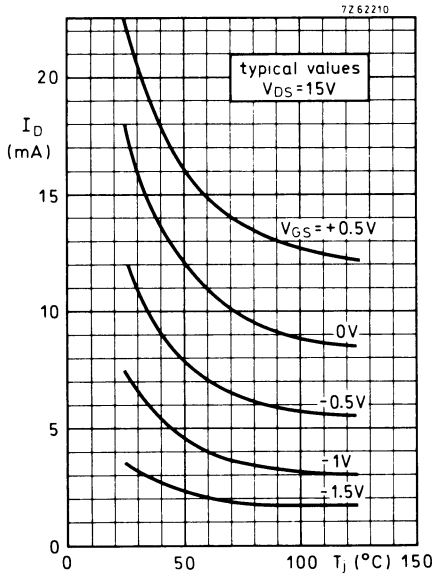
CHARACTERISTICS

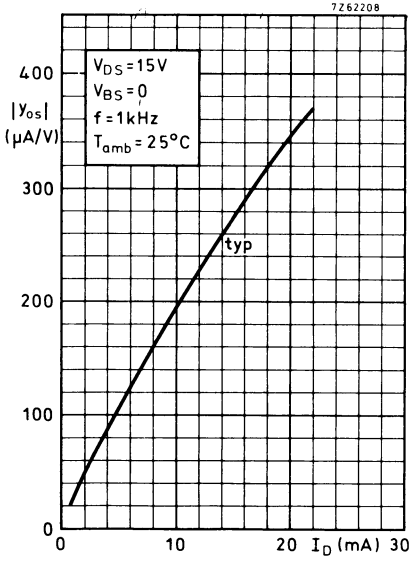
T_j = 25 °C unless otherwise specified

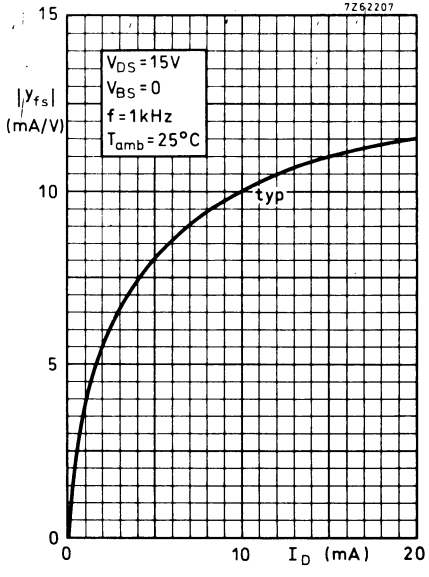
Gate currents; V_{BS} = 0				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 °C	I_{GSS}	<	200	pA
Bulk currents; V_{GB} = 0				
$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	µA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	µA
Drain current				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	10 to	40	mA
Gate-source voltage				
I_D = 100 nA; V_{DS} = 15 V	$-V_{GS}$	0.5 to	3.5	V
Gate-source cut-off voltage				
I_D = 100 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	<	4	V
y parameters				
I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C				
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	6	mS
Output admittance at f = 1 kHz	$\|y_{os}\|$	<	0.4	mS
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF
Noise figure at f = 200 MHz				
I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C				
G_S = 1 mS; B_S = B_{Sopt}	F	<	5	dB
Equivalent noise voltage T_{amb} = 25 °C				
I_D = 5 mA; V_{DS} = 15 V; f = 120 Hz	$V_n/\sqrt{B}$	typ.	300	nV/$\sqrt{Hz}$
T_{amb} = 25 °C f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	nV/$\sqrt{Hz}$
f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	nV/$\sqrt{Hz}$

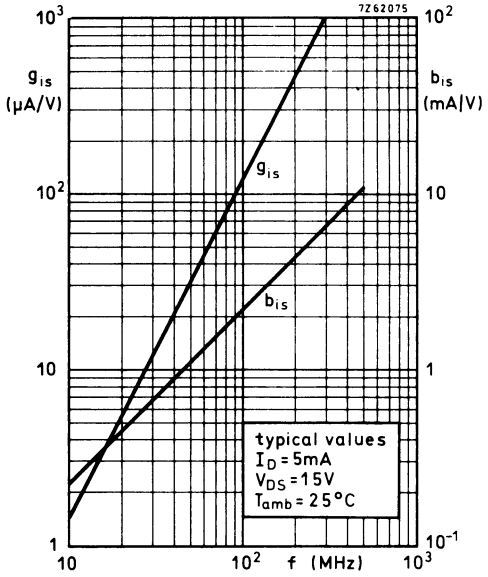

7Z62279
I_D (mA)
V_{BS} = 0
T_{amb} = 25°C
typ. values
V_{GS} = +0.5V
0V
-0.5V
-1V
-1.5V
V_{DS}=15V
V_{BS}=0
T_{amb}=25°C
d
g
b
s
20
15
10
5
0
-5
V_{GS} (V)
-2.5
0
5
10
15
V_{DS} (V)
20

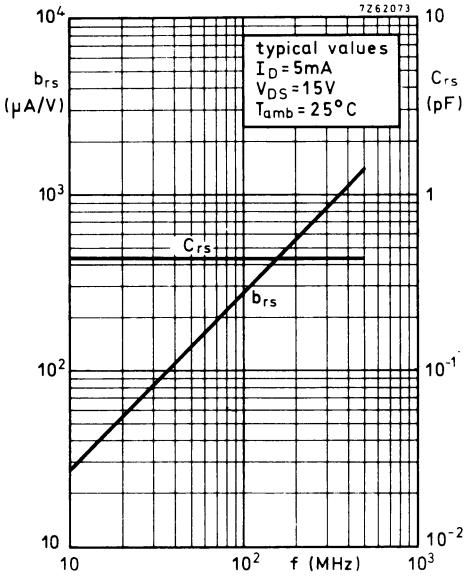

7Z62278
I_D (mA)
V_{BS} = +2V
+1V
0V
-1V
-2V
-3V
-5V
-7V
V_{DS}=15V
T_{amb}=25°C
typical values
d
g
b
s
20
15
10
5
0
-2.5
-2
-1.5
-1
-0.5
0
V_{GS} (V)
0.5

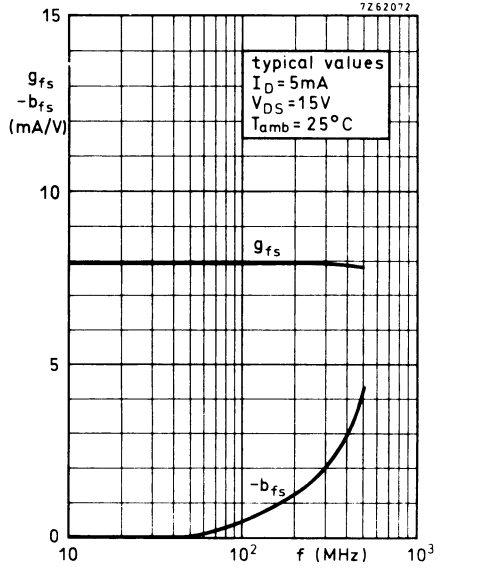

7Z62210
typical values
V_{DS}=15V
I_D (mA)
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
T_j (°C)

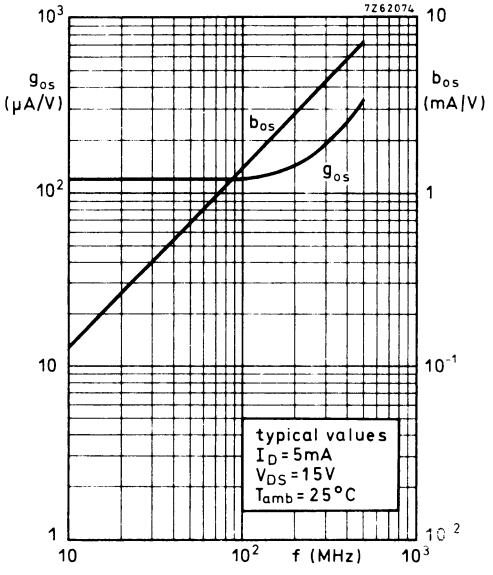

7Z62208
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{os}|$ (μA/V)
typ
I_D (mA)

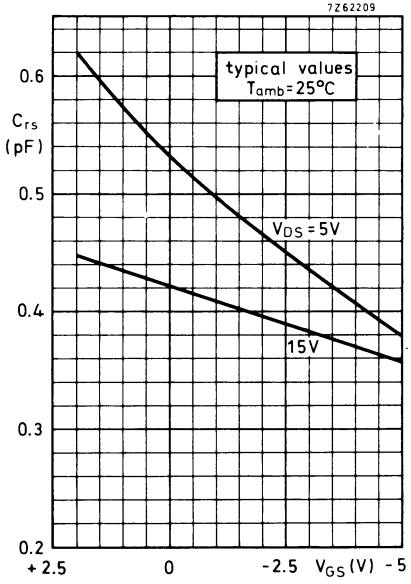

7Z62207
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{fs}|$ (mA/V)
typ
I_D (mA)

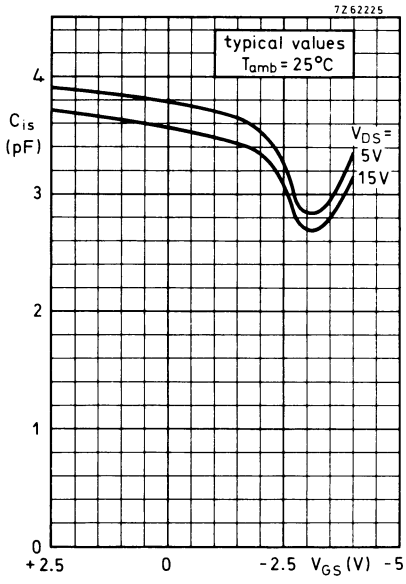

7Z62075
10^3
g_{is} (μA/V)
10^2
10
1
10^2
b_{is} (mA/V)
10
1
10^{-1}
g_{is}
b_{is}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
10
10^2 f (MHz) 10^3


7Z62073
10^4
b_{rs} (μA/V)
10^3
10^2
10
10
C_{rs} (pF)
1
10^{-1}
10^{-2}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
C_{rs}
b_{rs}
10
10^2 f (MHz) 10^3


7Z62072
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
10
10^2 f (MHz) 10^3


7Z62074
10^3
g_{os} (μA/V)
10^2
10
1
10
b_{os} (mA/V)
1
10^{-1}
10^{-2}
b_{os}
g_{os}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
10
10^2 f (MHz) 10^3


7Z62209
typical values
T_{amb} = 25°C
C_{rs} (pF)
0.6
0.5
0.4
0.3
0.2
V_{DS} = 5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5


7Z62225
typical values
T_{amb} = 25°C
C_{is} (pF)
4
3
2
1
0
V_{DS} =
5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	+15 −30	+15 −40	V V
Drain current (DC)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275		mW
Junction temperature	T_j	max.	125		°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	<	30		Ω
Feedback capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6		pF

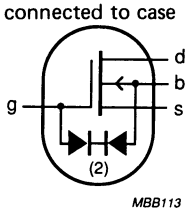
MECHANICAL DATA

Dimensions in mm

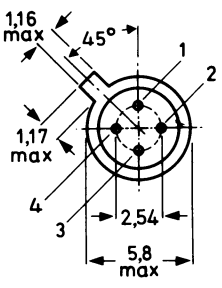
Fig. 1 TO-72.

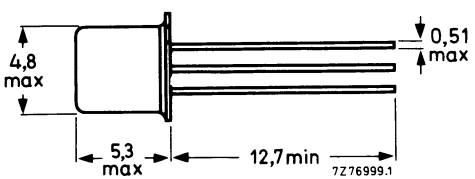
Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b) connected to case



MBB113





Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	+15 −15	+15 −15	V V
Gate-source voltage	V_{GS}	max.	+15 −30	+15 −40	V V
Drain current (DC)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275		mW
Storage temperature	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	125		°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD10	BSD12	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1,0		nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	<	10		nA
Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_S = 20 mA	g_{fs}	> typ.	10 15		mS mS

Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	<	2,0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0 V_{GS} = 5 V	r_{DSon}	typ. <	25 Ω 50 Ω
V_{GS} = 10 V	r_{DSon}	typ. <	15 Ω 30 Ω
Capacitances at f = 1 MHz (see Fig. 2) V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	2,3 pF
Output capacitance	C_{oss}	typ.	1,9 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 to + 5 V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

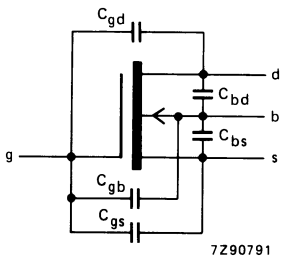


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$
$C_{oss} = C_{gd} + C_{bd}$
$C_{rss} = C_{gd}$

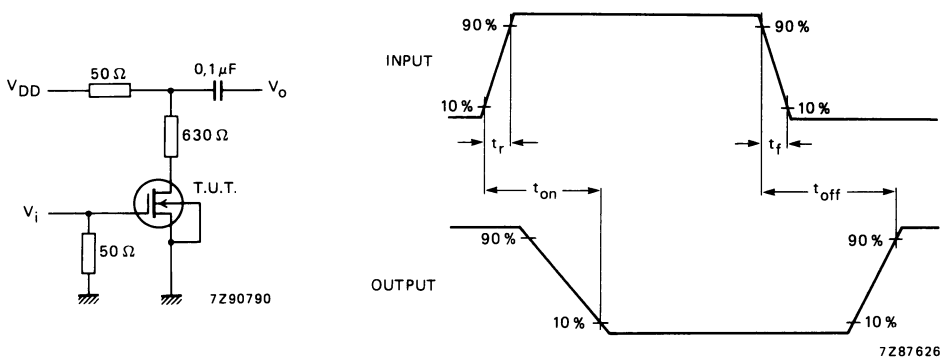


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; t_r < 0,5 ns; t_f < 1,0 ns; t_p = 20 ns; δ < 0,01.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistors of the N-channel depletion mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

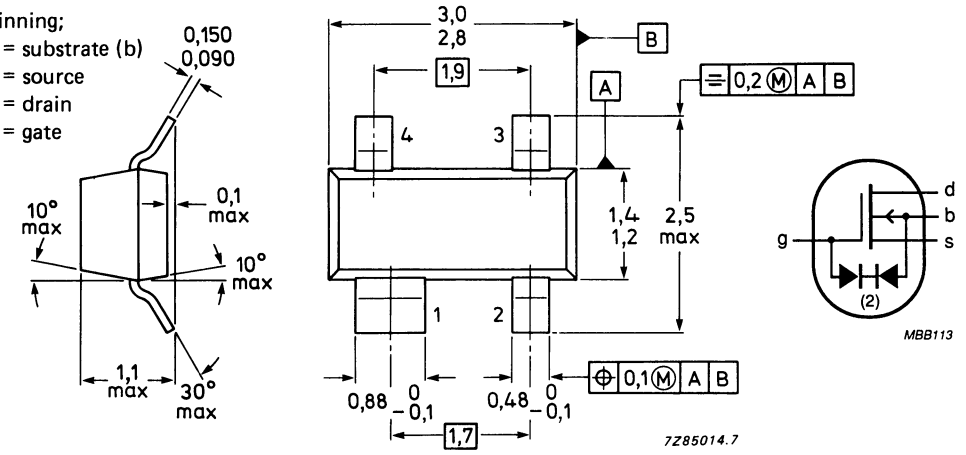
			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	+15 −30	+15 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230		mW
Junction temperature	T_j	max.	125		°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	<	30		Ω
Feed-back capacitance $V_{GS} = V_{BS}$ = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate



TOP VIEW

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	± 15	± 25	V
Gate-source voltage	V_{GS}	max.	+ 15 −30	+ 15 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230		mW
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	125		°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD20	BSD22	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10V	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD}$ = 5 V; V_{SD} = 10V	I_{SDoff}	typ.	1,0		nA
Gate-substrate leakage current → $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	<	10		nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	> typ.	10 mS 15 mS
Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I I_D = 10 μA	$-V_{(P)GS}$	<	2,0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 5 V	R_{DSon}	typ. <	25 Ω 50 Ω
V_{GS} = 10 V	R_{DSon}	typ. <	15 Ω 30 Ω
Capacitances at f = 1 MHz V_{GS} = V_{BS} = −5V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on} t_{off}	typ. typ.	1,0 ns 5,0 ns

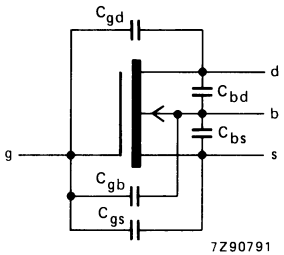
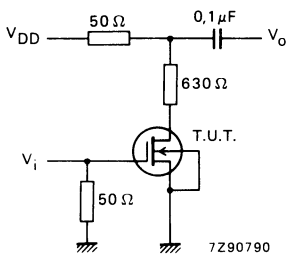


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



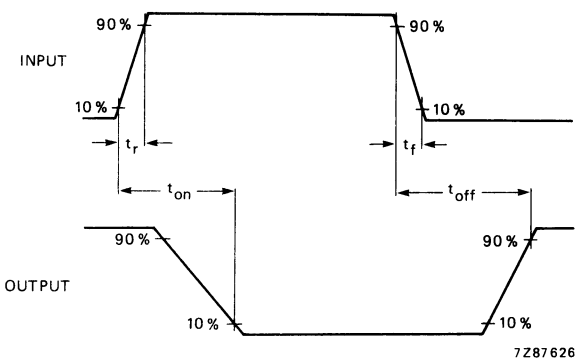


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; t_r < 0,5 ns; t_f < 1,0 ns; t_p = 20 ns; δ < 0,01.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Drain-source resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 15 V	$R_{DS(on)}$	typ.		25			Ω
Feedback capacitance V_{GS} = V_{BS} = −15 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.		0,6			pF
Junction temperature	T_j	max.		125			°C

MECHANICAL DATA

See next page.

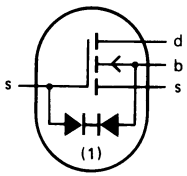
MECHANICAL DATA

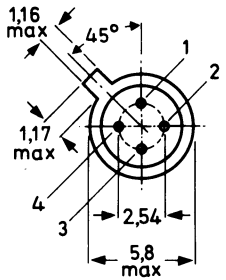
Dimensions in mm

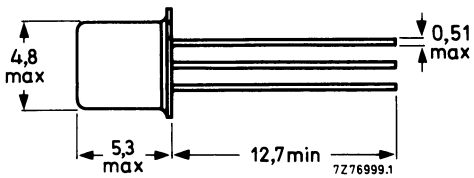
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b) connected to case







(1) Diode protection on types BSD213 and BSD215 only.
BSD212 and BSD214 have no protection diode.
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Storage temperature range	T_{stg}			−65 to + 175			°C
Junction temperature	T_j	max.		125			°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage							
$V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	>	10	10	20	20	V
Source-drain breakdown voltage							
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	10	20	20	V
Drain-substrate breakdown voltage							
V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	15	25	25	V
Source-substrate breakdown voltage							
V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	>	15	15	25	25	V
Drain-source leakage current							
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1,0	1,0	–	–	nA
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 20 V	I_{DSoff}	typ.	–	–	1,0	1,0	nA
Source-drain leakage current							
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1,0	1,0	–	–	nA
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 20 V	I_{SDoff}	typ.	–	–	1,0	1,0	nA
Gate-substrate leakage current							
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 40 V	I_{GBS}	<	0,1	–	0,1	–	nA
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	<	–	10	–	10	nA
Threshold voltage							
$V_{DS} = V_{GS} = V_{GS(th)}$; V_{SB} = 0; I_S = 1 μA	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance							
I_D = 1,0 mA; V_{SB} = 0;							
V_{GS} = 5 V	$R_{DS(on)}$	typ.	50	50	50	50	Ω
		<	70	70	70	70	Ω
V_{GS} = 10 V	$R_{DS(on)}$	typ.	30	30	30	30	Ω
		<	45	45	45	45	
V_{GS} = 15 V	$R_{DS(on)}$	typ.	25	25	25	25	Ω
V_{GS} = 25 V	$R_{DS(on)}$	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz				
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	typ.	15	mS
		>	10	
Capacitance at f = 1 MHz (see Fig. 2)				
$V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

DYNAMIC CHARACTERISTICS (continued)

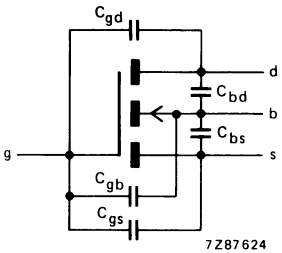


Fig. 2 Capacitances model.

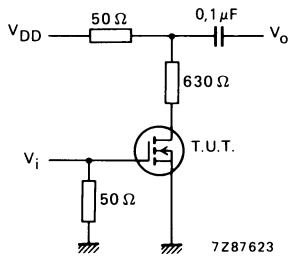
$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

Switching times (see Fig. 3)

V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns



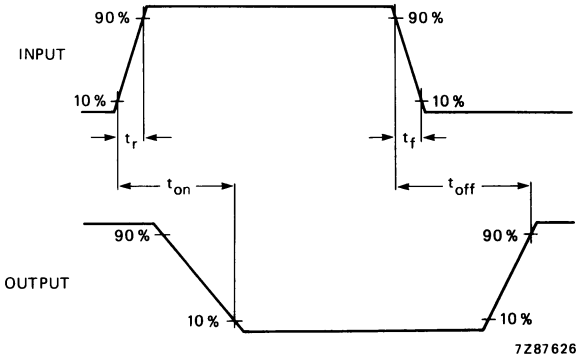


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

R_i = 50 Ω

t_r < 0,5 ns

t_f < 1,0 ns

t_p = 20 ns

δ < 0,01

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

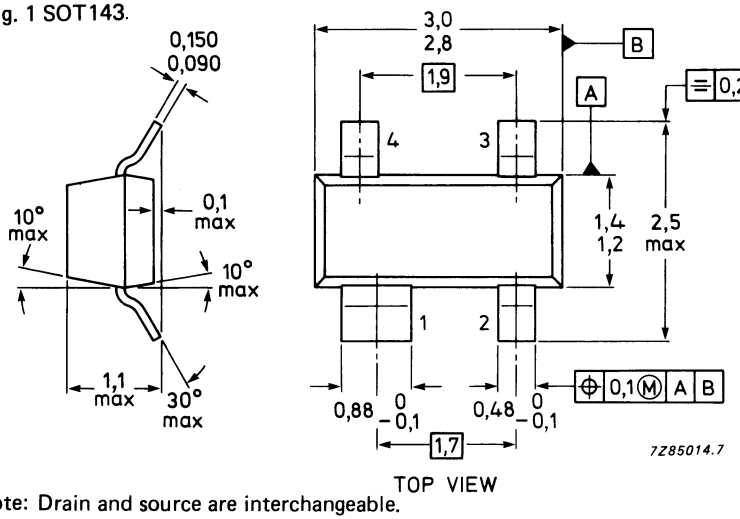
Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Gate-source threshold voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu A$	$V_{GS(th)}$	$>$ $<$	0.1 2.0	V V
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 0.1 mA	R_{DSon}	$<$	45	Ω
Feed-back capacitance $V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

MECHANICAL DATA

SOT143 (see Fig. 1).

See also *Soldering recommendations*.

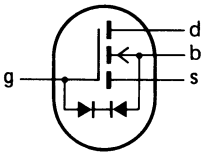
Fig. 1 SOT143.



Dimensions in mm

Marking code:
BSS83 = M74

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	V
Source-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15	V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current			
$V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6{,}6$ V	I_{SDoff}	<	10 nA
Forward transconductance at f = 1 kHz			
$V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	>	10 mS
		typ.	15 mS
Gate-source threshold voltage			
$V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu$A	$V_{GS(th)}$	>	0,1 V
		<	2,0 V
Drain-source ON-resistance			
$I_D = 0{,}1$ mA;			
$V_{GS} = 5$ V; $V_{SB} = 0$	R_{DSon}	<	70 Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	R_{DSon}	<	45 Ω
$V_{GS} = 3{,}2$ V; $V_{SB} = 6{,}8$ V (see Fig. 4)	R_{DSon}	typ.	80 Ω
		<	120 Ω
Gate-substrate zener voltages			
$V_{DB} = V_{SB} = 0$; $-I_C = 10\ \mu$A	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB} = 0$; $+I_G = 10\ \mu$A	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz			
$V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2)			
$V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Pulse generator:

R_i = 50 Ω
t_r < 0,5 ns
t_f < 1,0 ns
t_p = 20 ns
δ < 0,01

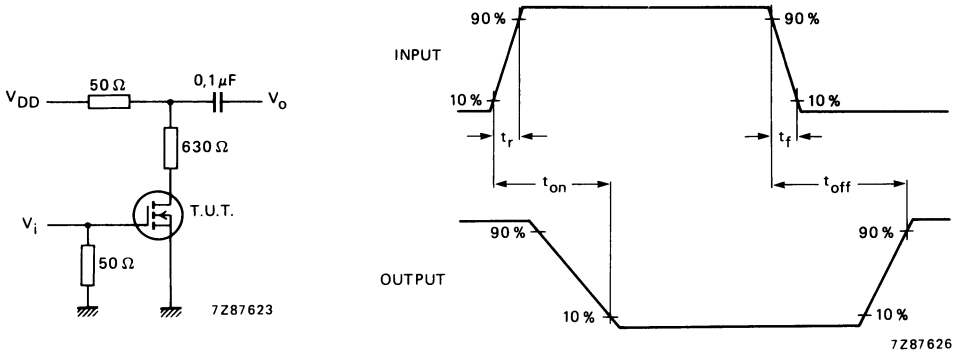


Fig. 2 Switching times test circuit and input and output waveforms.

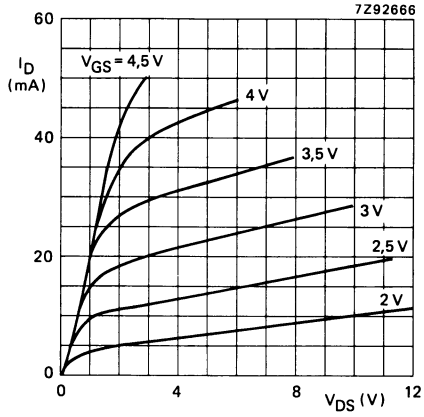


Fig. 3 V_{SB} = 0; typical values.

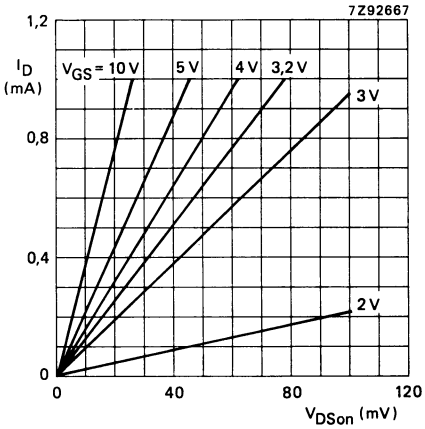


Fig. 4 V_{SB} = 6,8 V; typical values.

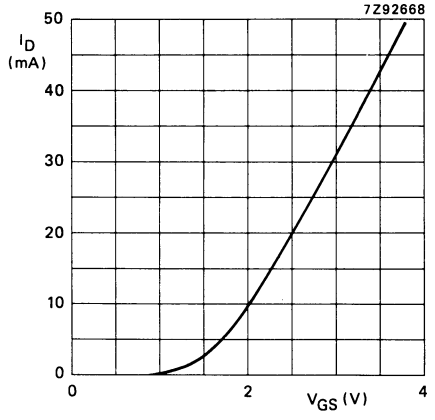


Fig. 5 V_{DS} = 10 V; V_{BS} = 0; typical values.

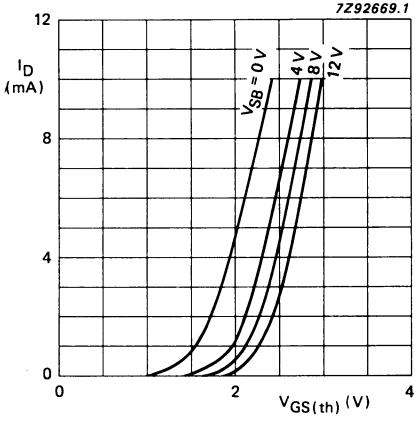


Fig. 6 $V_{DS} = V_{GS} = V_{GS(th)}$.

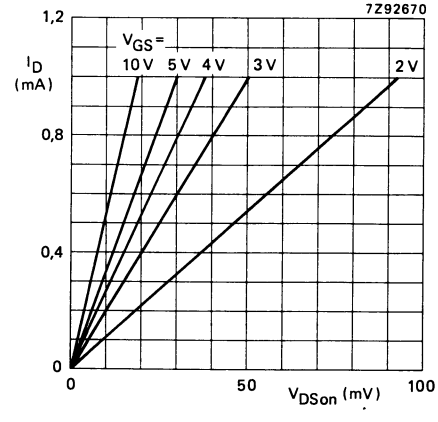


Fig. 7 V_{SB} = 0; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
T_j = 25 °C.

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

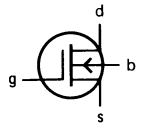
Drain-source resistance (on) at f = 1 kHz			
V_{DS} = 0; V_{GS} = 5 V; V_{BS} = 0	$R_{ds\ on}$	<	50 Ω
Drain-source resistance (off)			
V_{DS} = 10 V; $-V_{GS}$ = 5 V; V_{BS} = 0	$R_{DS\ off}$	>	10 GΩ
Feedback capacitance at f = 1 MHz			
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	<	0,5 pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	<	0,5 pF

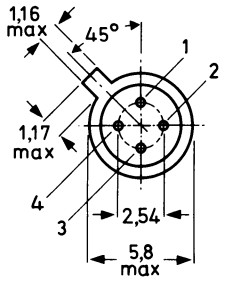
MECHANICAL DATA

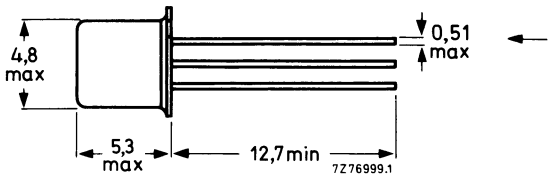
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	V_{GB}	max. min.	10 V −10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 V −15 V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	V_{G-N}	max. min.	50 V −50 V
→ Drain current (DC)	I_D	max.	25 mA
Drain current (peak value) $t_r = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50 mA
Source current (peak value) $t_r = 20$ ms; $\delta = 0{,}1$	I_{SM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 125 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

→ From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain cut-off currents; V_{BS} = 0.

V_{DS} = 10 V; $-V_{GS}$ = 5 V	I_{DSX}	<	1	nA
V_{DS} = 10 V; $-V_{GS}$ = 5 V; T_j = 125 °C	I_{DSX}	<	1	µA

Source cut-off currents; V_{BD} = 0

V_{SD} = 10 V; $-V_{GD}$ = 5 V	I_{SDX}	<	1	nA
V_{SD} = 10 V; $-V_{GD}$ = 5 V; T_j = 125 °C	I_{SDX}	<	1	µA

Gate currents; V_{BS} = 0

$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 °C	I_{GSS}	<	200	pA

Bulk currents; V_{GB} = 0

$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	µA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	µA

Drain-source resistance (on) at f = 1 kHz; V_{BS} = 0

V_{GS} = 0 ; V_{DS} = 0	$R_{ds\ on}$	<	100	Ω
V_{GS} = 0 ; V_{DS} = 0; T_j = 125 °C	$R_{ds\ on}$	<	150	Ω
$+V_{GS}$ = 5 V; V_{DS} = 0	$R_{ds\ on}$	<	50	Ω

Drain-source resistance (off)

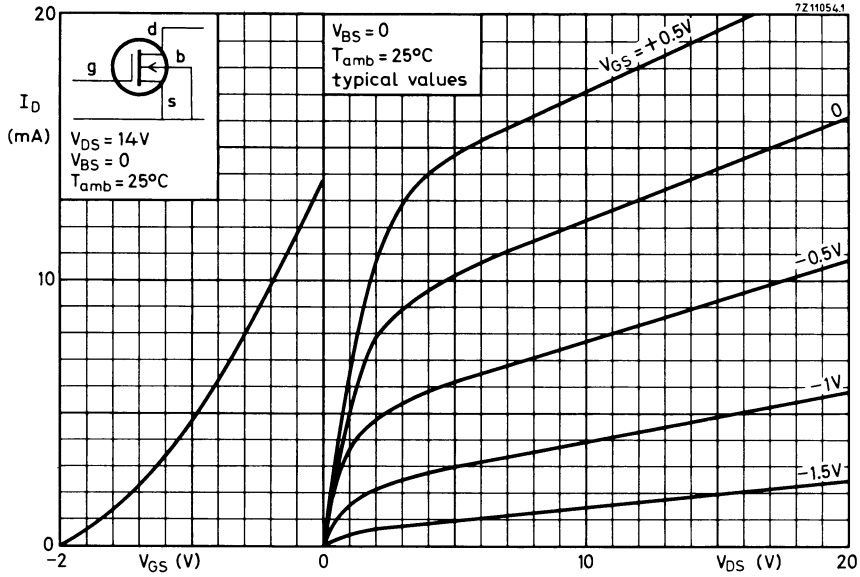
$-V_{GS}$ = 5 V; V_{DS} = 10 V; V_{BS} = 0	$R_{DS\ off}$	>	10	GΩ

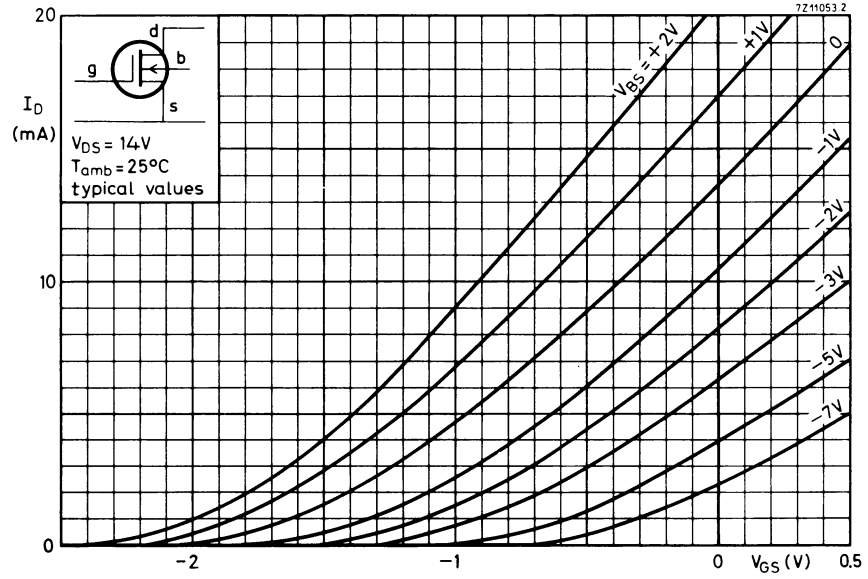
Feedback capacitances at f = 1 MHz

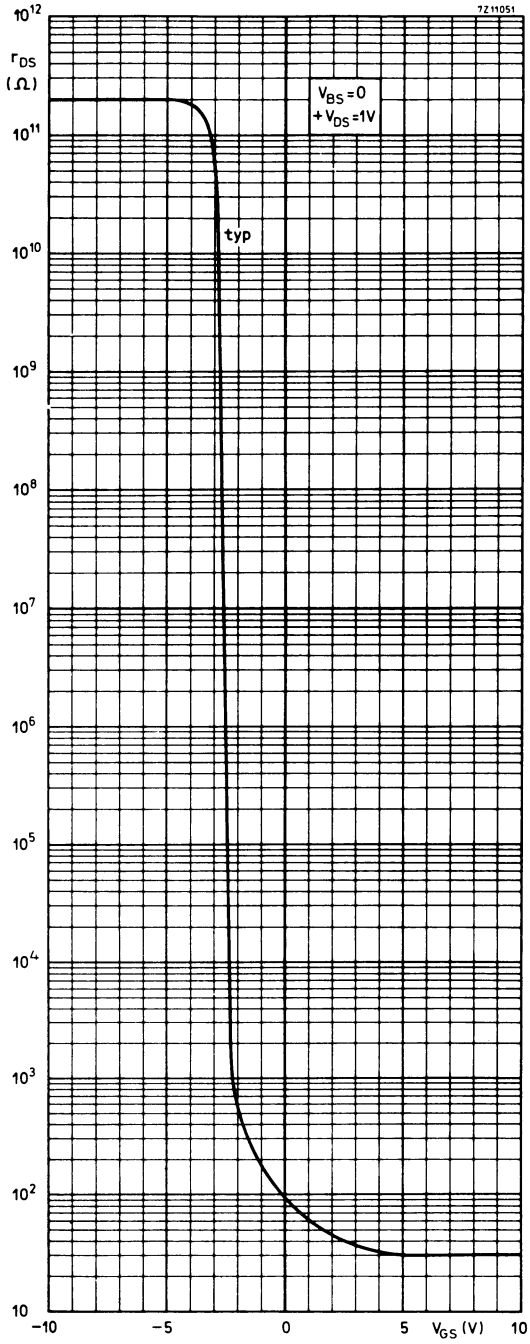
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	<	0,5	pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	<	0,5	pF

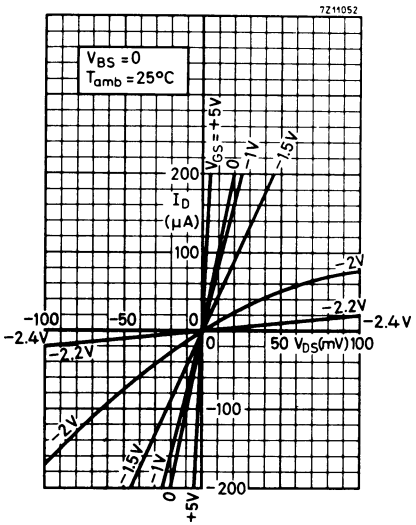
Gate to all other terminals capacitance at f = 1 MHz

$-V_{GB}$ = 5 V; V_{SB} = V_{DB} = 0	$C_{g\text{-}n}$	<	6	pF


7Z11054.1
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
V_{BS} = 0
T_{amb} = 25°C
V_{BS} = 0
T_{amb} = 25°C
typical values
V_{GS} = +0.5V
0
−0.5V
−1V
−1.5V
−2
V_{GS} (V)
0
10
V_{DS} (V)
20


7Z11053.2
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
T_{amb} = 25°C
typical values
V_{BS} = +2V
+1V
0
−1V
−2V
−3V
−5V
−7V
−2
−1
0
V_{GS} (V)
0.5


7Z11051
r_{DS} (Ω)
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
V_{BS} = 0
$+V_{DS}$ = 1V
typ
−10
−5
0
5
10
V_{GS} (V)


7Z11052
V_{BS} = 0
T_{amb} = 25°C
V_{GS} = +5V
0
−1V
−1.5V
−2V
−2.2V
−2.4V
200
I_D (μA)
100
−100
−50
0
50
100
V_{DS}(mV)
−200
+5V

DEVICE DATA
MOS-FETs
dual gate

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8 dB

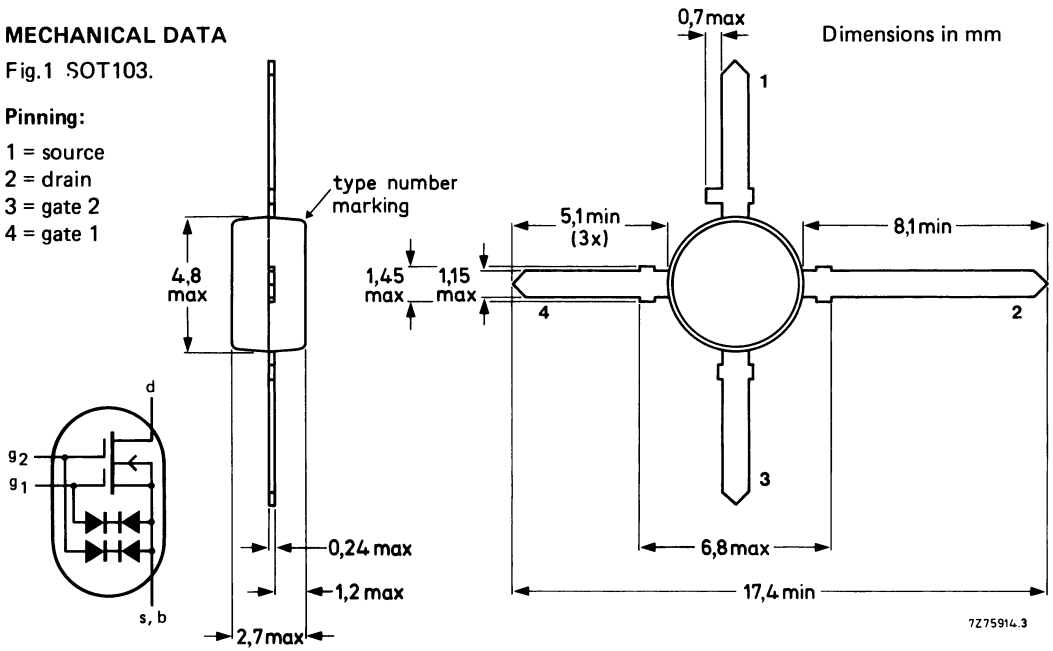
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

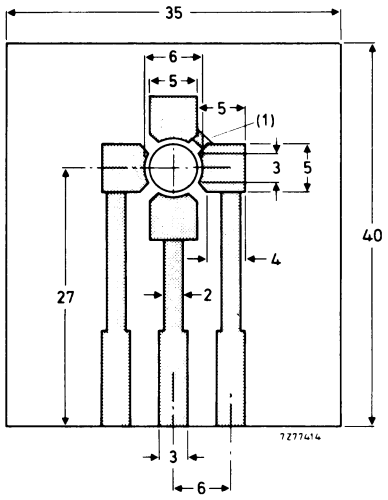
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board	$R_{th\ j-a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt			
G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	23 dB
G_L = 1 mS; $B_L = B_L$ opt; f = 800 MHz	G_p	typ.	16.5 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF	←
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

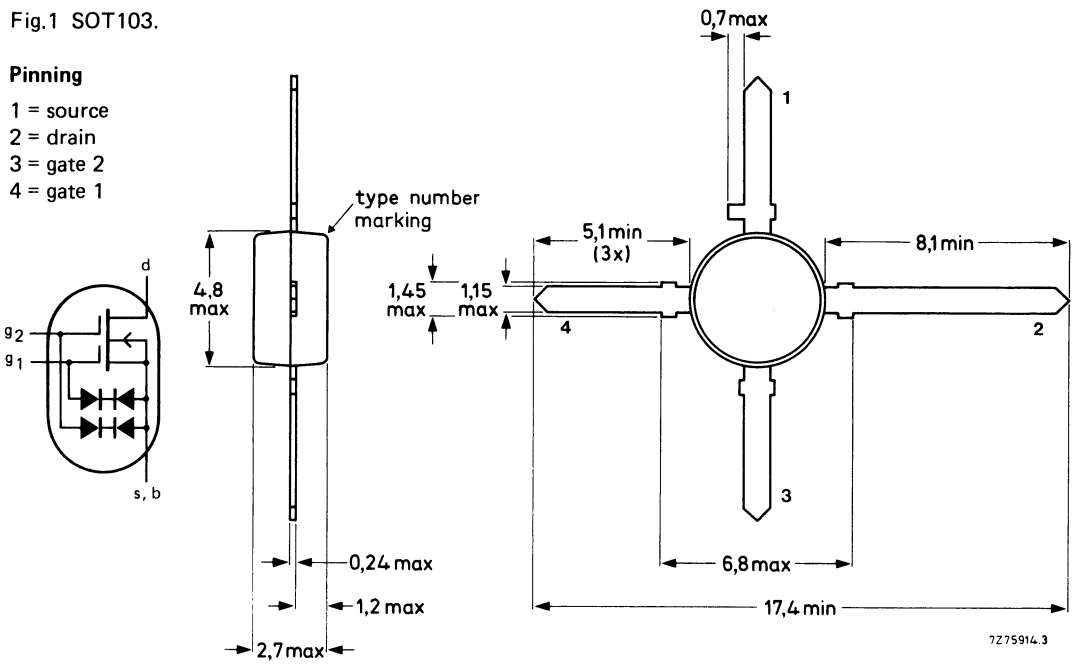
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

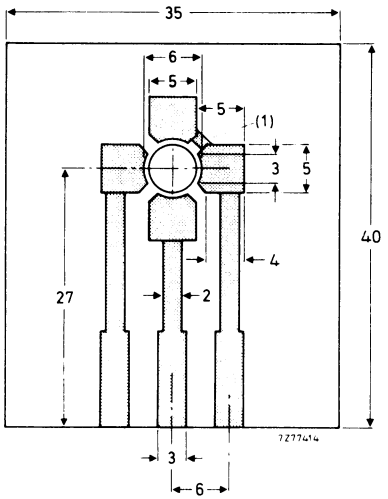
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6.0 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6.0 to 20 V
Drain current			
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.5 pF
		max.	3.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at G_S = 2 mS ; $B_S = B_S$ opt f = 200 MHz	F	typ.	1.0 dB
Power gain at G_S = 2 mS ; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

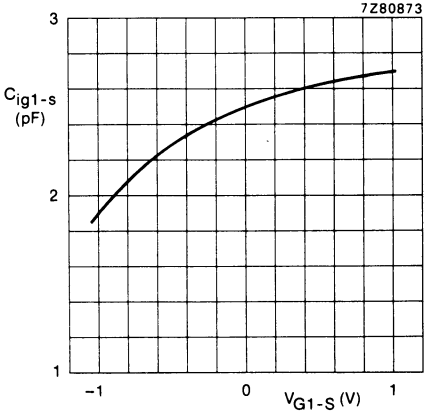


Fig. 3 V_{G2-S} = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

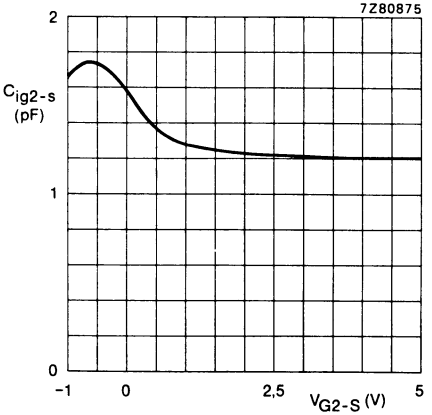


Fig. 4 V_{G1-S} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

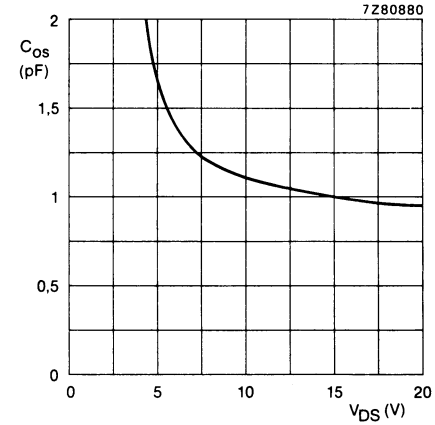


Fig. 5 V_{G2-S} = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

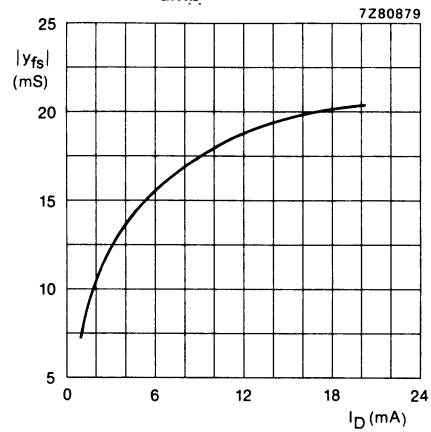


Fig. 6 V_{G2-S} = 4; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

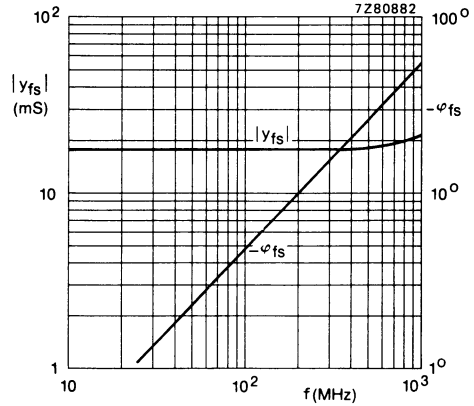


Fig. 7 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

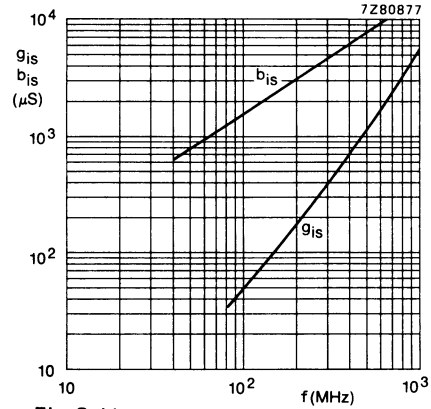


Fig. 8 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

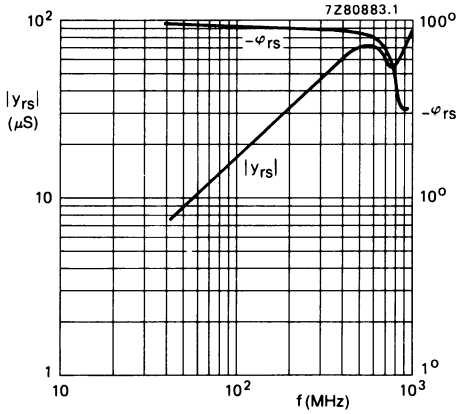


Fig. 9 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

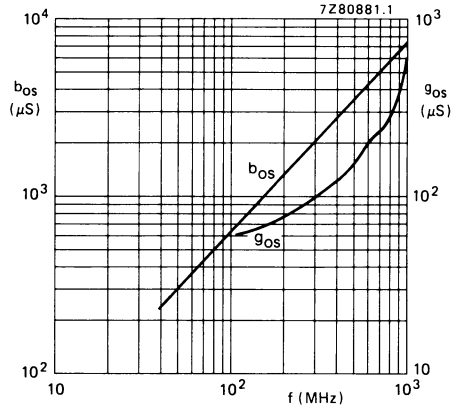


Fig. 10 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

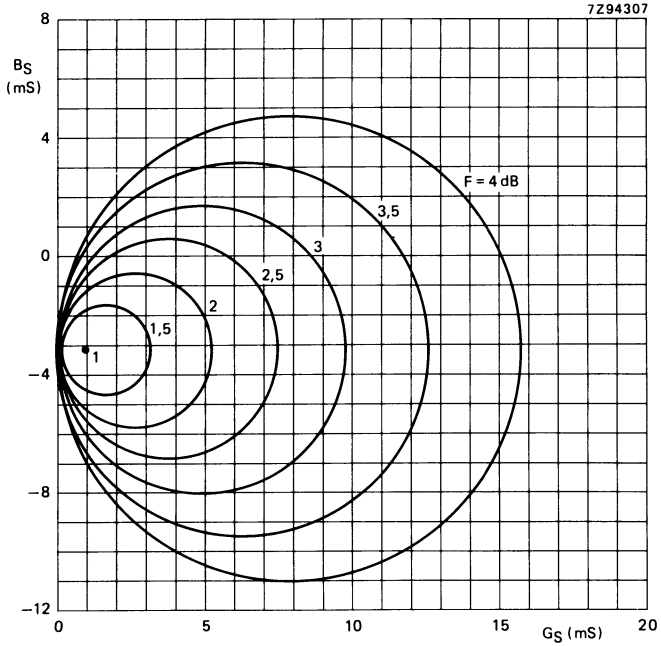


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

QUICK REFERENCE DATA

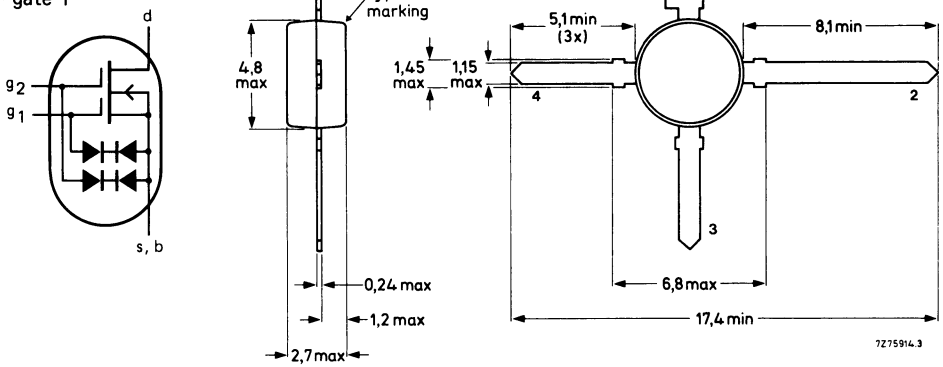
Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_{Sopt} I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,0 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT103.

Pinning
1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

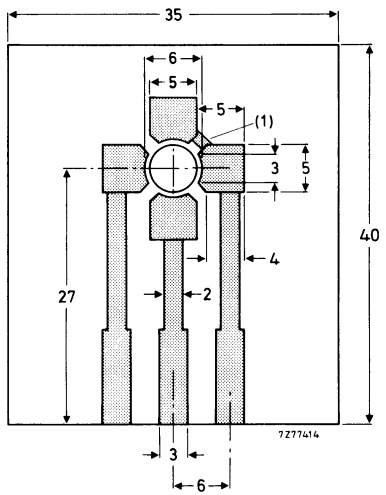
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (DC or average)	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on a printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless stated otherwise

Gate cut-off currents				
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	<	50	nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	<	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20	V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20	V
Drain current				
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2,0 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	<	2,5	V
I_D = 20 μA; V_{DS} = 15 V; + $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	<	2,0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	15	mS
		typ.	18	mS
Input capacitance at gate 1 at f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,5	pF
Input capacitance at gate 2 at f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0	pF
Noise figure at G_S = 2 mS; $B_S = B_{Sopt}$ and f = 200 MHz	F	typ.	1,0	dB
Power gain at G_S = 2 mS; $B_S = B_{Sopt}$ G_L = 0,5 mS; $B_L = B_{Lopt}$; f = 200 MHz	G_P	typ.	25	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF ← 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 3.3 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	1.8 dB

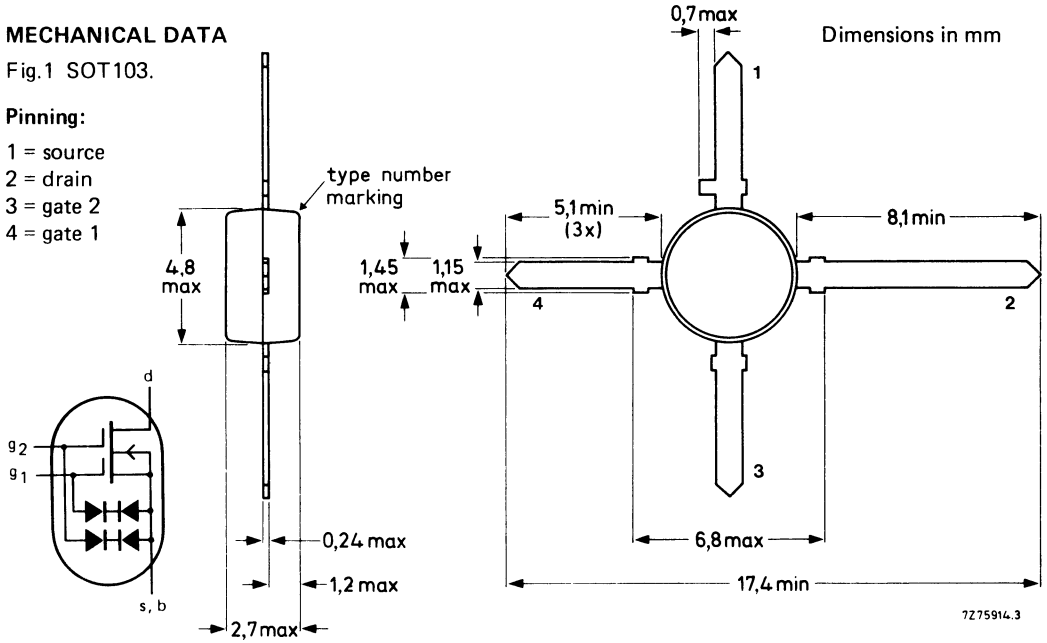
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



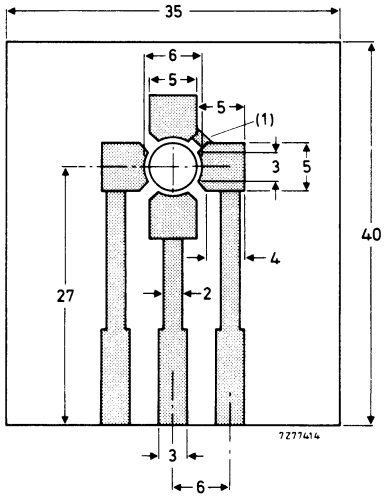
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335 K/W



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.3 pF 2.6 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
f = 800 MHz; G_S = 3.3 mS; $B_S = B_S$ opt	F	typ.	1.8 dB
Power gain			
f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS; B_S = opt; B_L = opt	G_p	typ.	25 dB
f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS; B_S = opt; B_L = opt	G_p	typ.	18 dB

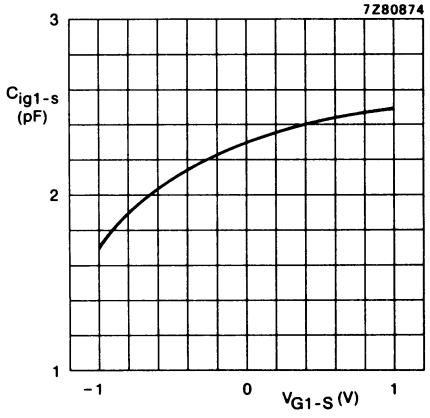


Fig.3 V_{G2-S} = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

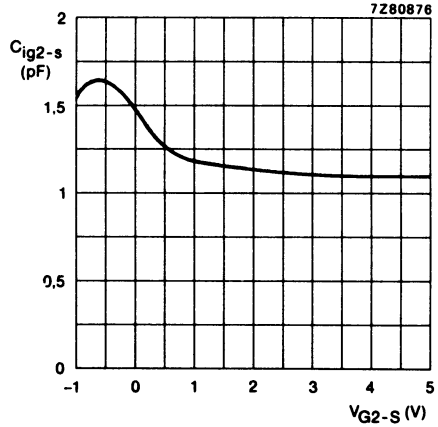


Fig.4 V_{G1-S} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

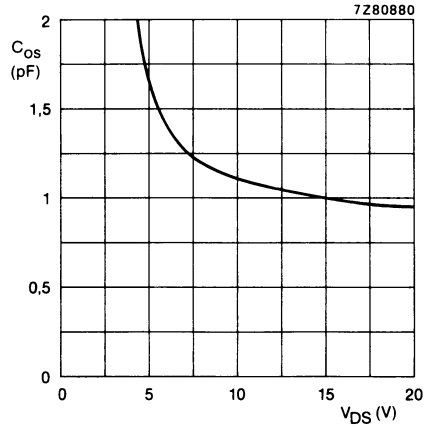


Fig. 5 $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

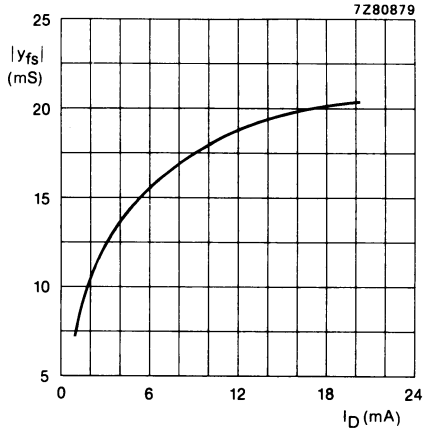


Fig. 6 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

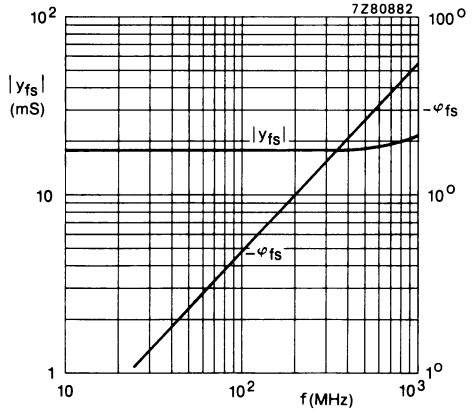


Fig. 7 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

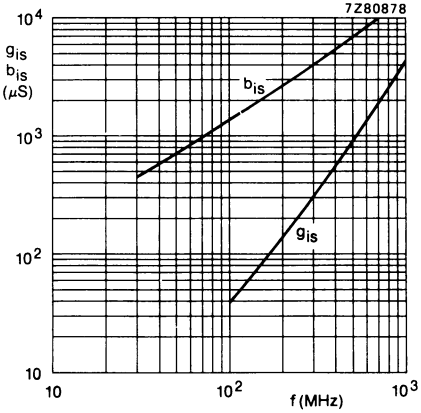


Fig. 8 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

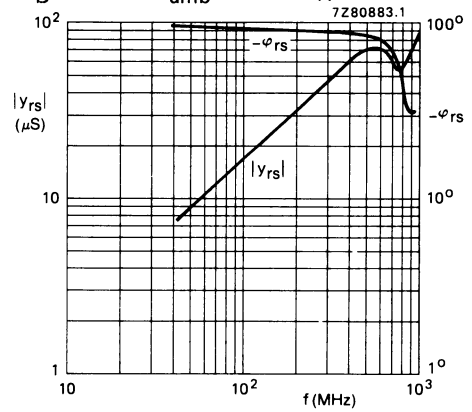


Fig. 9 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

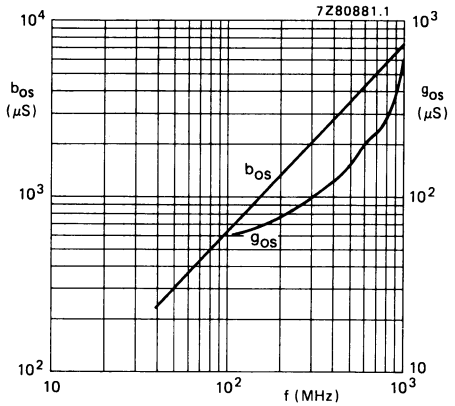


Fig. 10 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

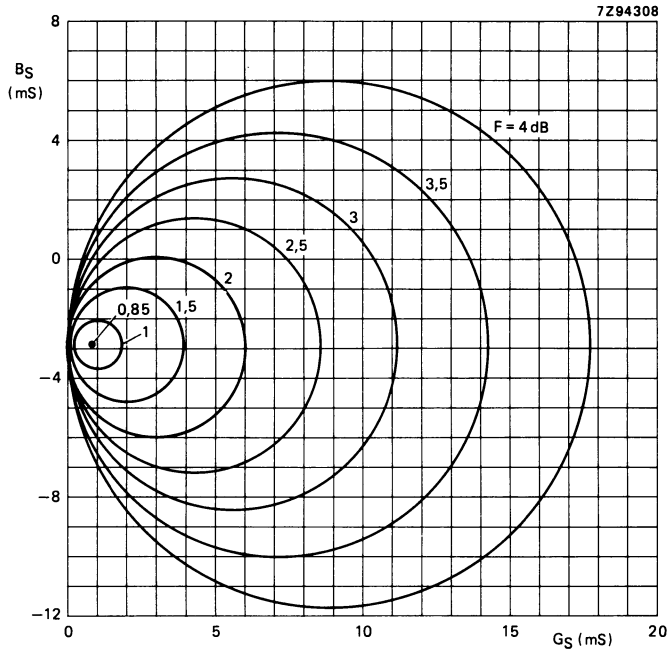


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; typical values.

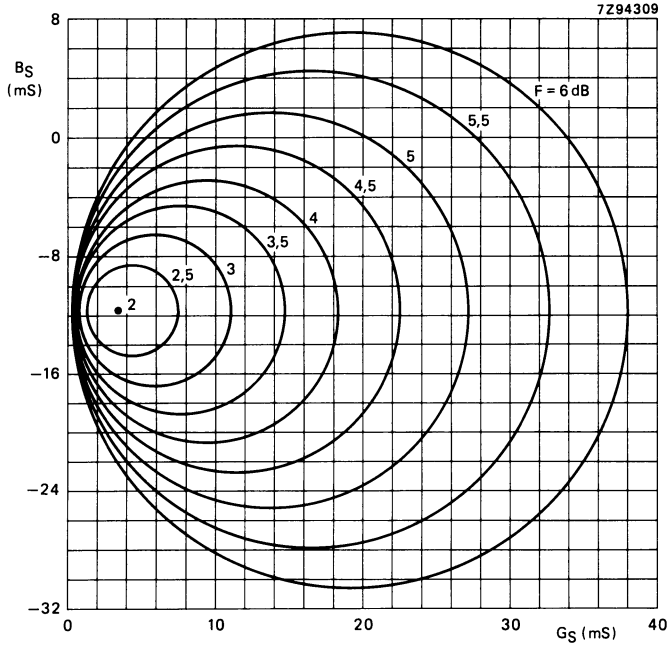


Fig. 12 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 800 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected. Intended for UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment.
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current (DC)	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.6 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 5 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0	dB

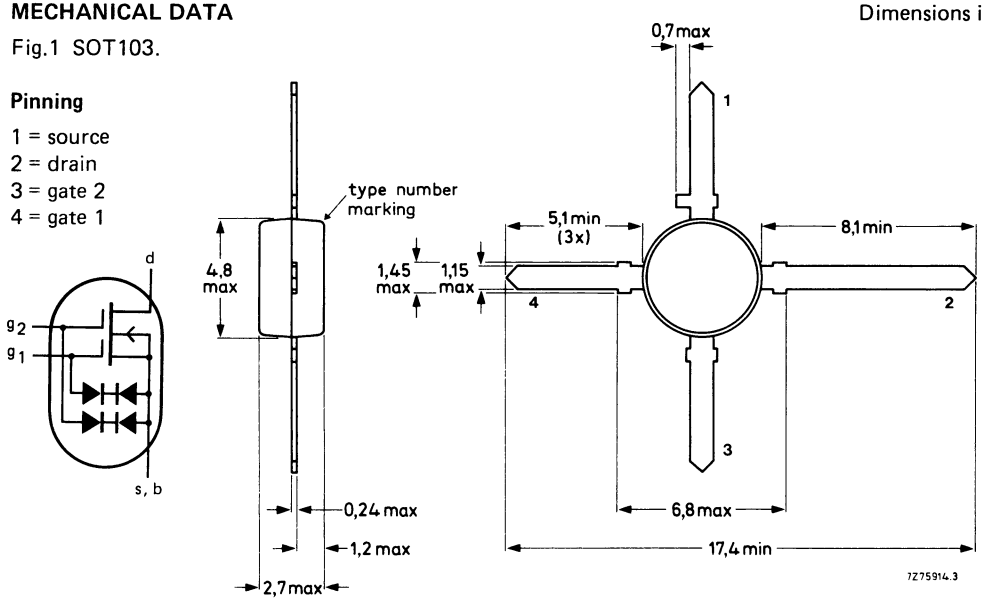
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

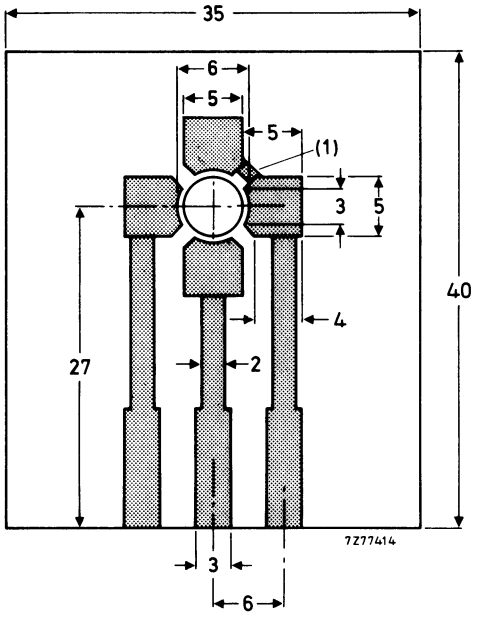
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 7 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	25 nA
± V_{G2-S} = 7 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	25 nA
Gate-source breakdown voltages			
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		8 to 20 V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	min.	0.2 V
		max.	1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	min.	0.2 V
		max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	18 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.6 pF
		max.	3.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
		max.	35 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.1 pF
Noise figure at f = 800 MHz; G_S = 5 mS; B_S = B_S opt	F	typ.	2.0 dB
		max.	3.0 dB

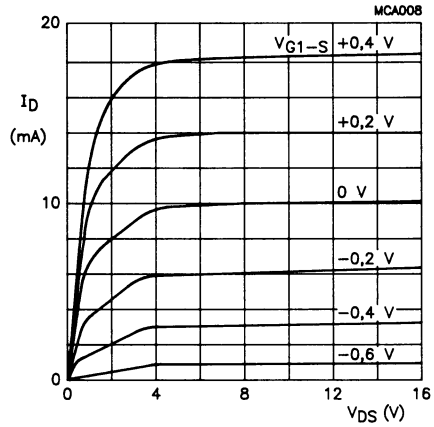


Fig.3 Output characteristics.
$V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

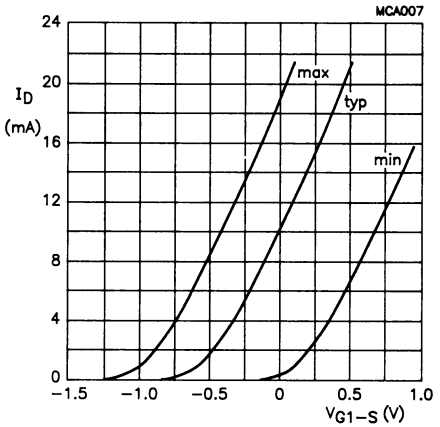


Fig.4 Transfer characteristics.
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

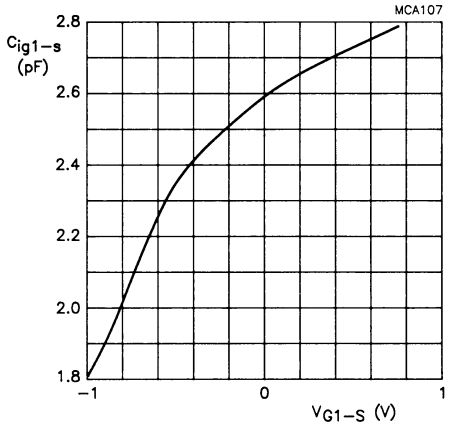


Fig.5 Gate 1 input capacitance as a function of gate 1 source voltage;
f = 1 MHz; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

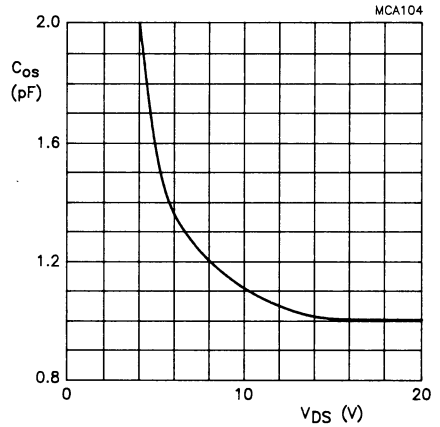


Fig.6 Output capacitance as a function of drain voltage; f = 1 MHz;
I_D = 10 mA; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

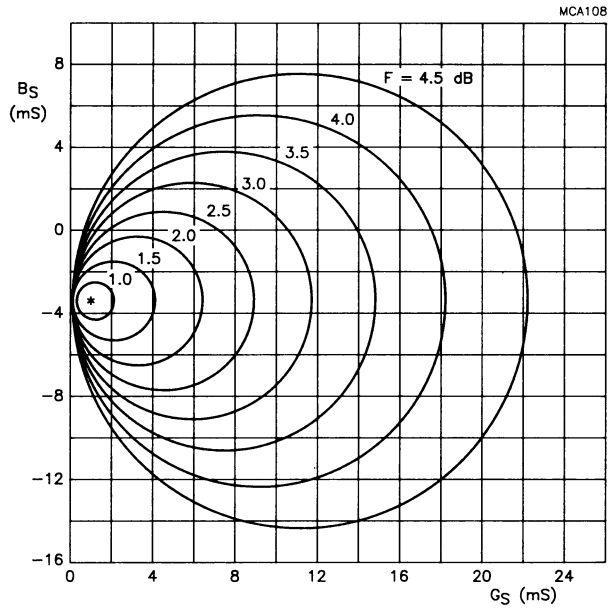


Fig.7 Circles of constant noise figures; f = 200 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

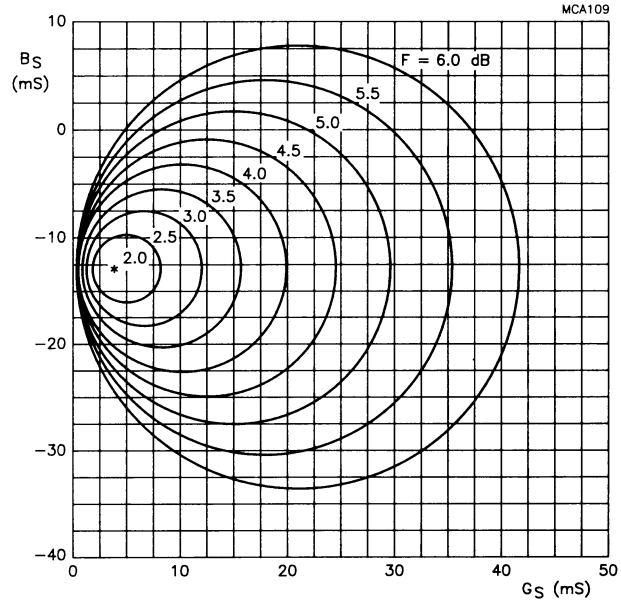


Fig.8 Circles of constant noise figures; f = 800 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

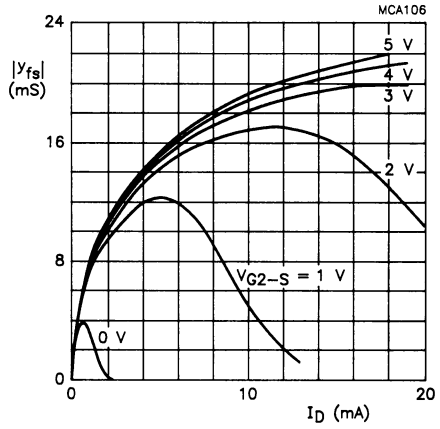


Fig.9 Forward transfer admittance as a function of drain current; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

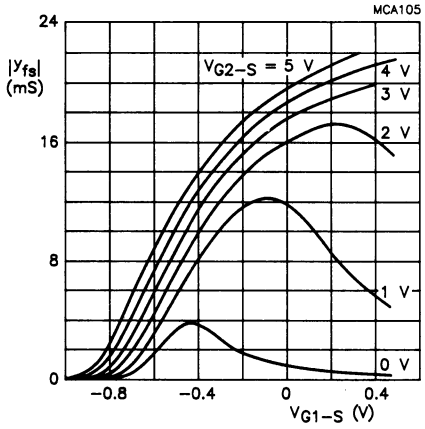


Fig.10 Forward transfer admittance as a function of gate 1 source voltage; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2.1	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0.7	dB

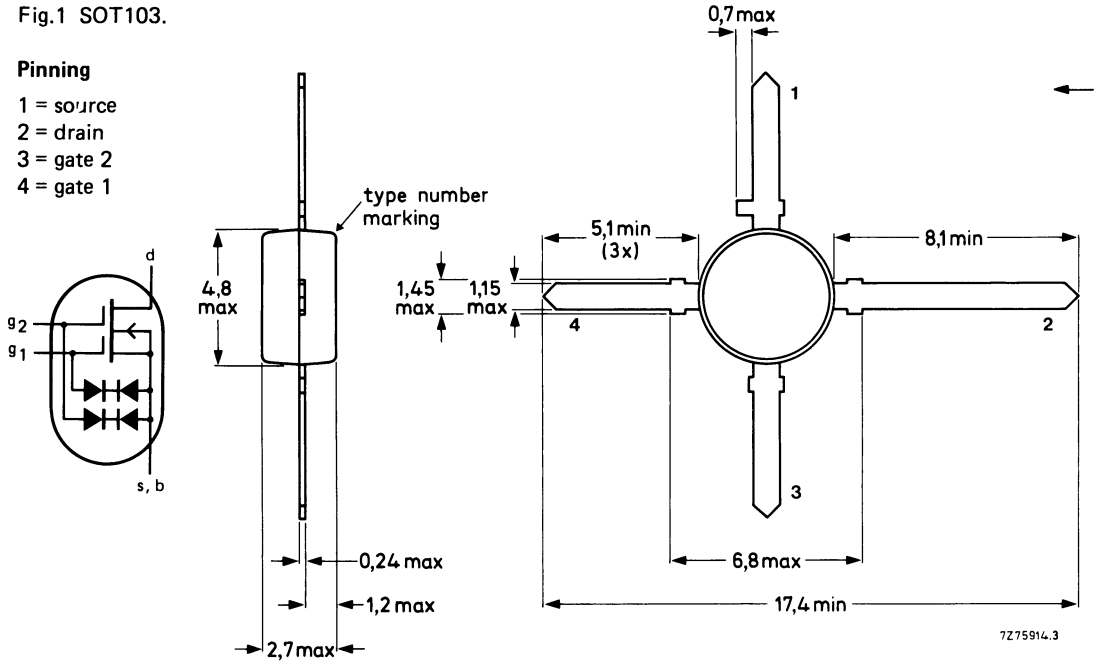
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



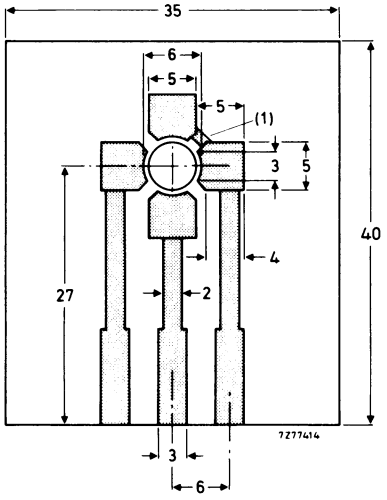
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335	K/W



Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents			
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	<	50 nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	<	50 nA
Gate-source breakdown voltages			
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$	6 to 20	V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$	6 to 20	V
Drain current			
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}	4 to 25	mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	< 2.5	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	< 2.5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> 10	mS
		typ. 14	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. 2.1	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ. 1.0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. 20	fF
Output capacitance at f = 1 MHz	C_{os}	typ. 1.1	pF
Noise figure at f = 100 MHz; G_S = 1 mS; B_S = B_S opt	F	typ. 0.7	dB
		< 1.7	dB
Noise figure at f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ. 1.0	dB
		< 2.0	dB
Transducer gain at f = 100 MHz; G_S = 1 mS; B_S = B_S opt; G_L = 0.5 mS; B_L = B_L opt	G_{tr}	typ. 29	dB
Transducer gain at f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0.5 mS; B_L = B_L opt	G_{tr}	typ. 26	dB

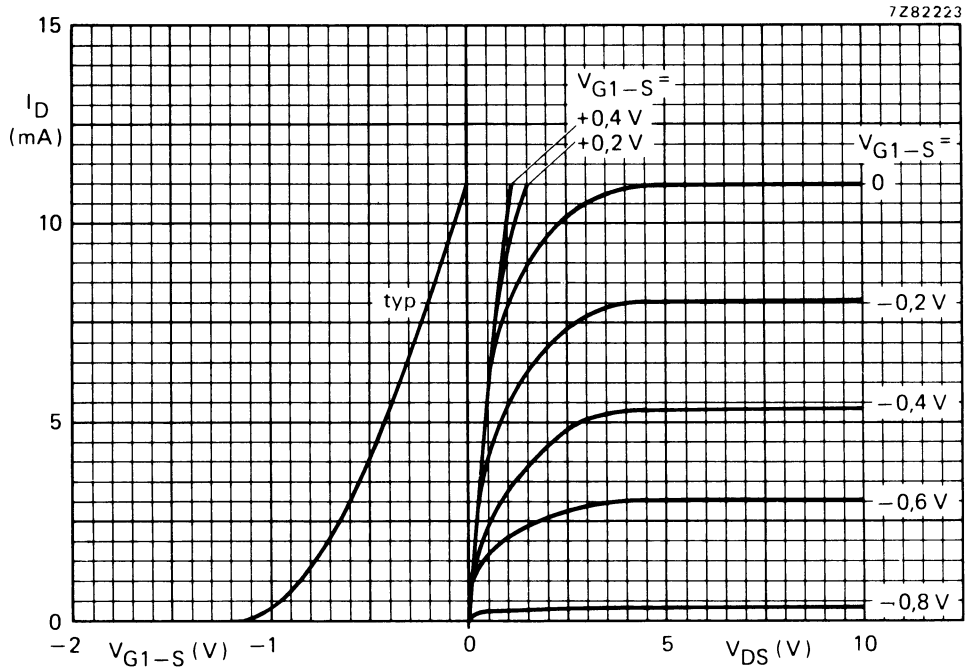


Fig. 3 **Left-hand graph:** V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C. **Right-hand graph:** V_{G2-S} = + 4 V; T_{amb} = 25 °C.

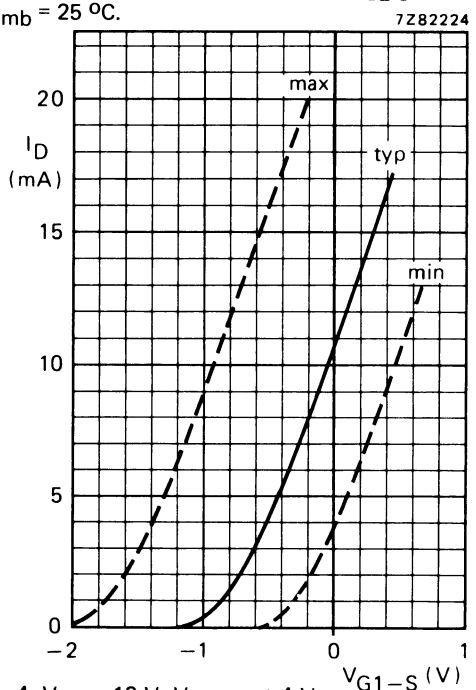


Fig. 4 V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

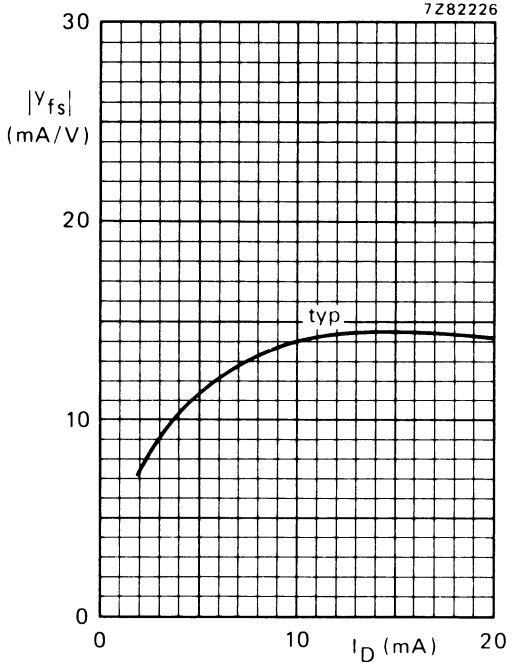


Fig. 5 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 kHz; T_{amb} = 25 °C.

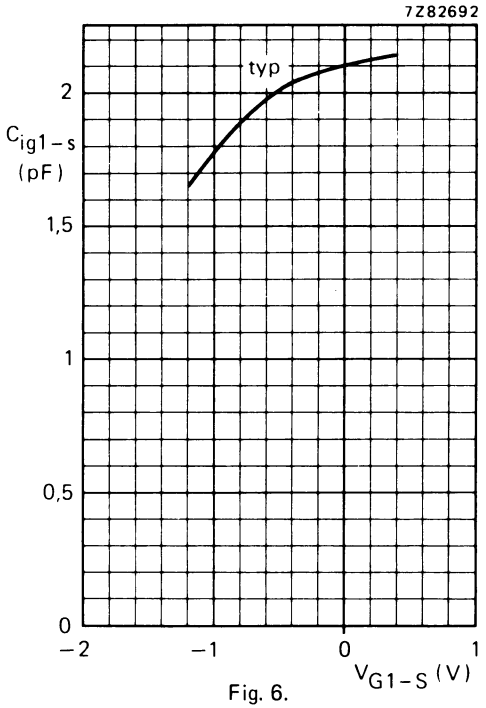


Fig. 6.

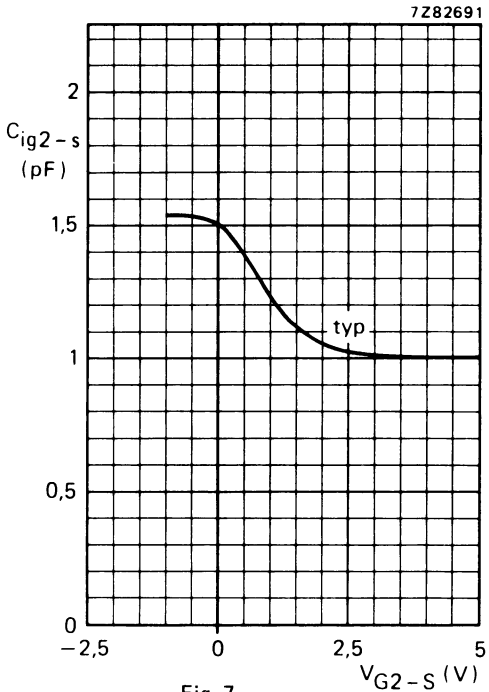


Fig. 7.

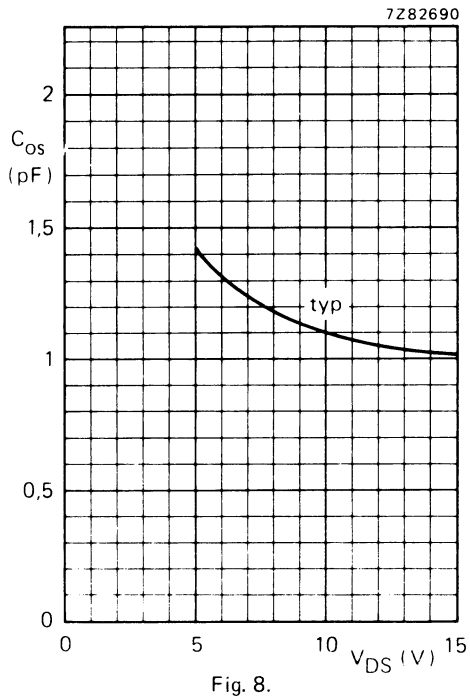


Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

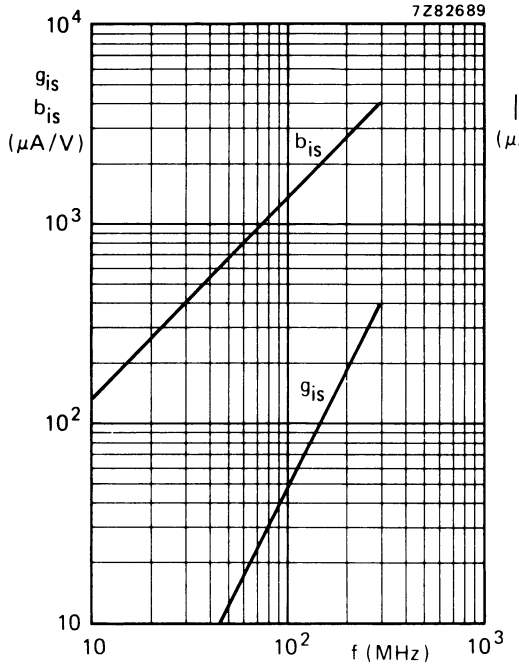


Fig. 9.

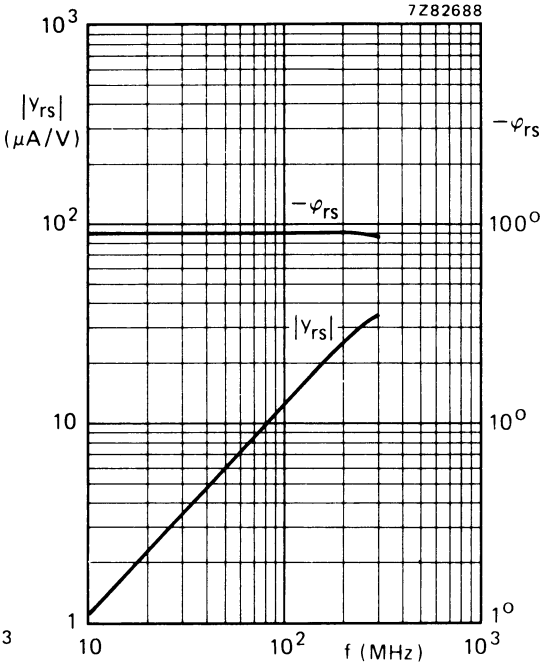


Fig. 10.

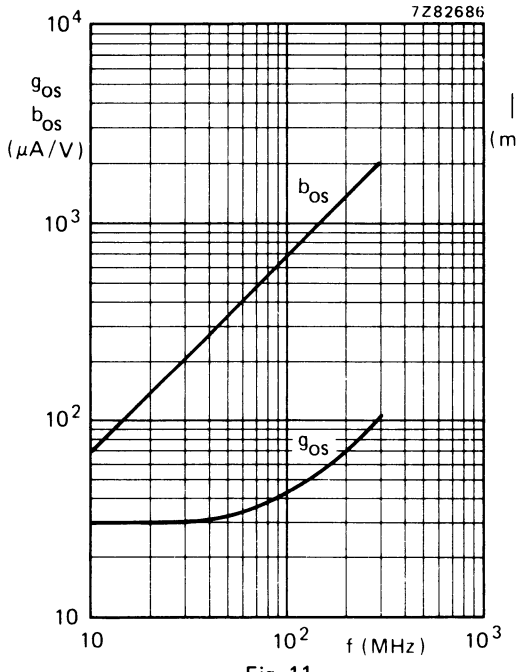


Fig. 11.

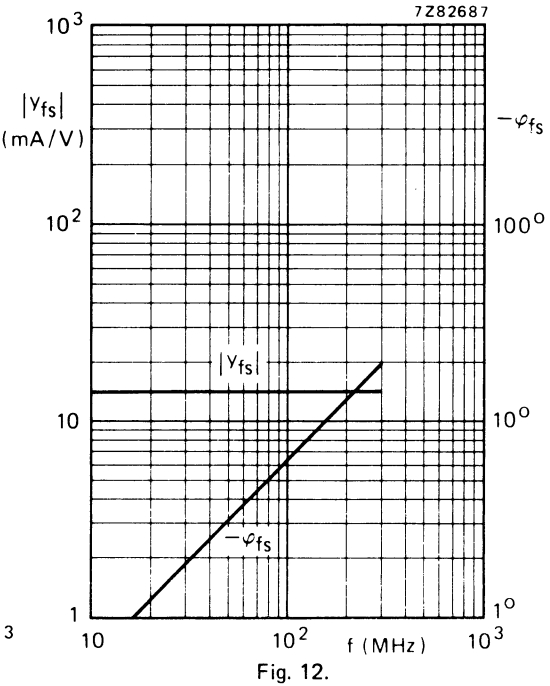


Fig. 12.

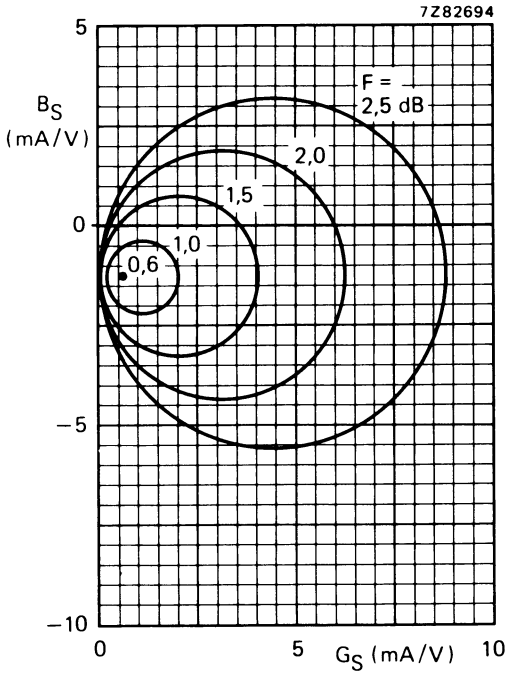


Fig. 13 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 100 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

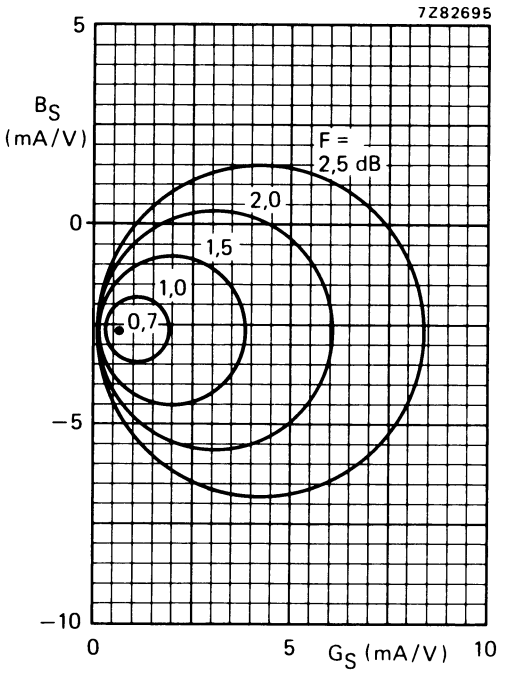


Fig. 14 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

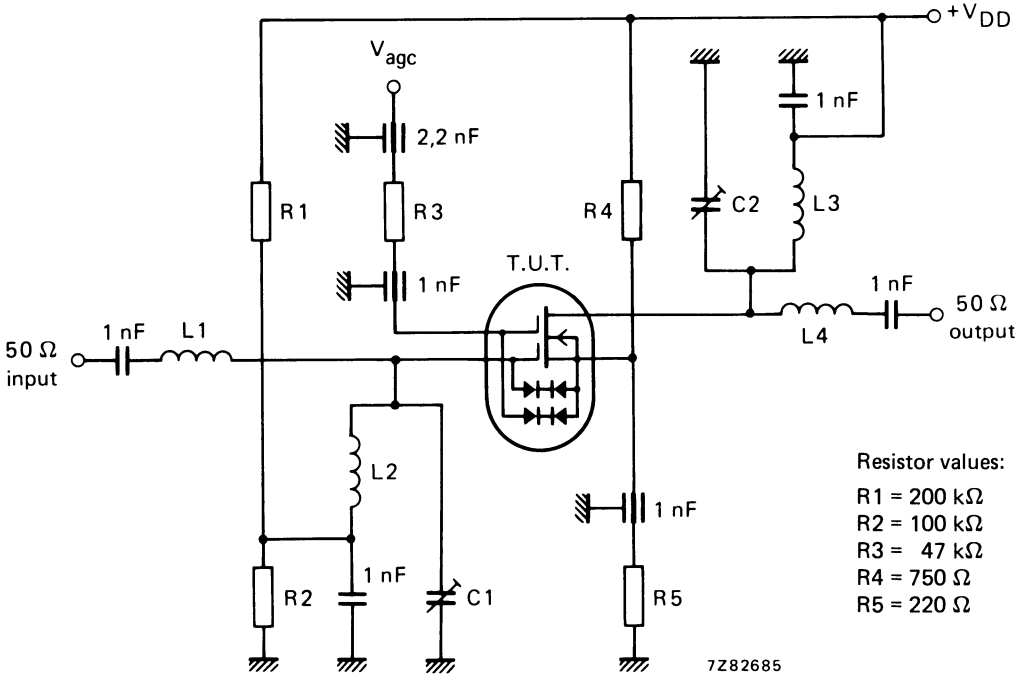


Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

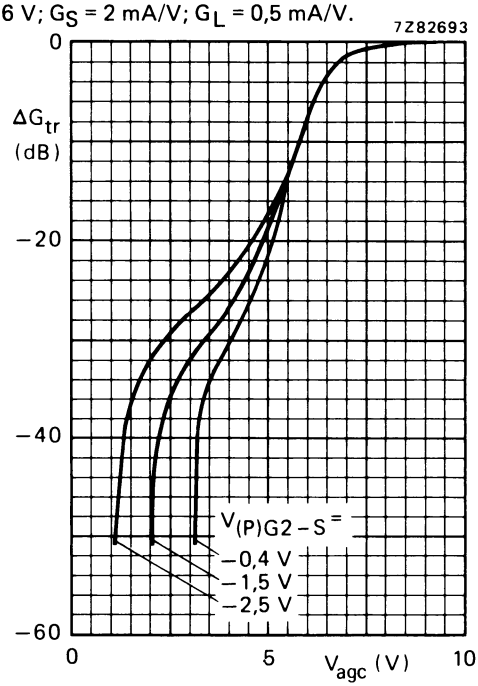


Fig. 16 V_{DD} = 16 V; f = 200 MHz;
T_{amb} = 25 °C; typical values;
see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4.0	pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2	dB

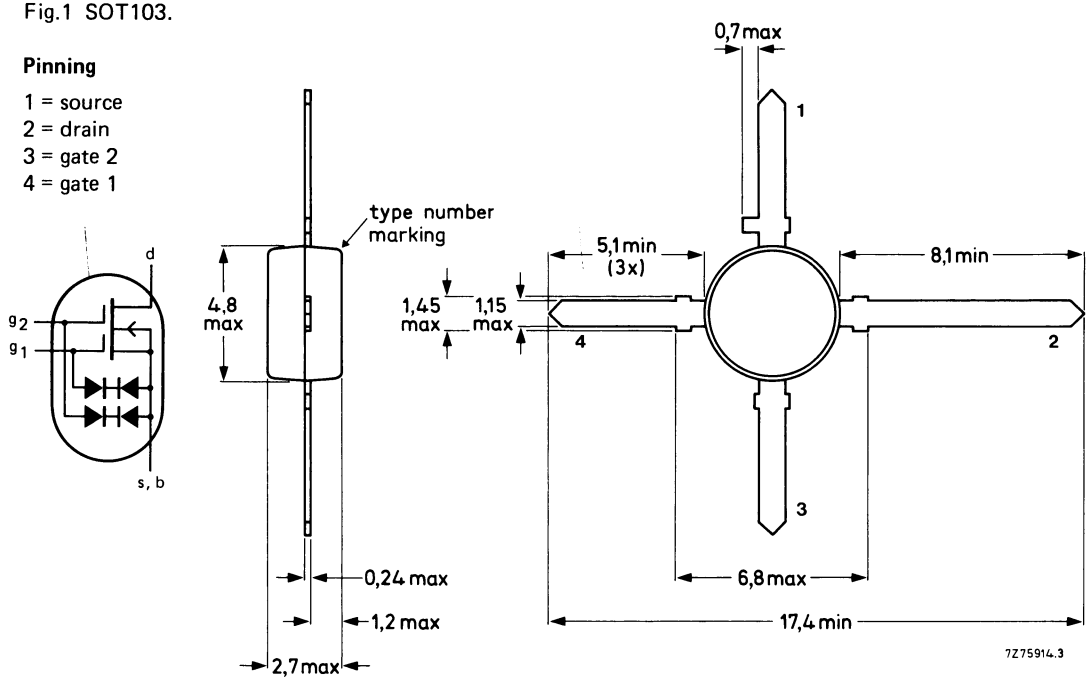
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

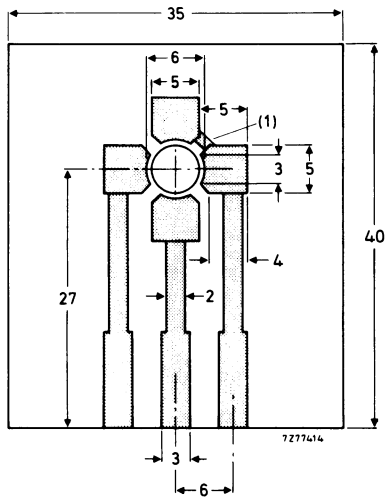
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents

$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm I_{G1\text{-}SS}$	<	25	nA
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm I_{G2\text{-}SS}$	<	25	nA

Gate-source breakdown voltages

$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G1\text{-}SS}$	>	8 to 20	V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G2\text{-}SS}$	>	8 to 20	V

Gate-source cut-off voltages

I_D = 20 μA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	<	1.3	V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	<	1.1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	20	mS
		typ.	25	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4.0	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.7	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2.0	pF
Noise figure at f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1.2	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	12	mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8	pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8	dB

MECHANICAL DATA

Fig.1 SOT143.

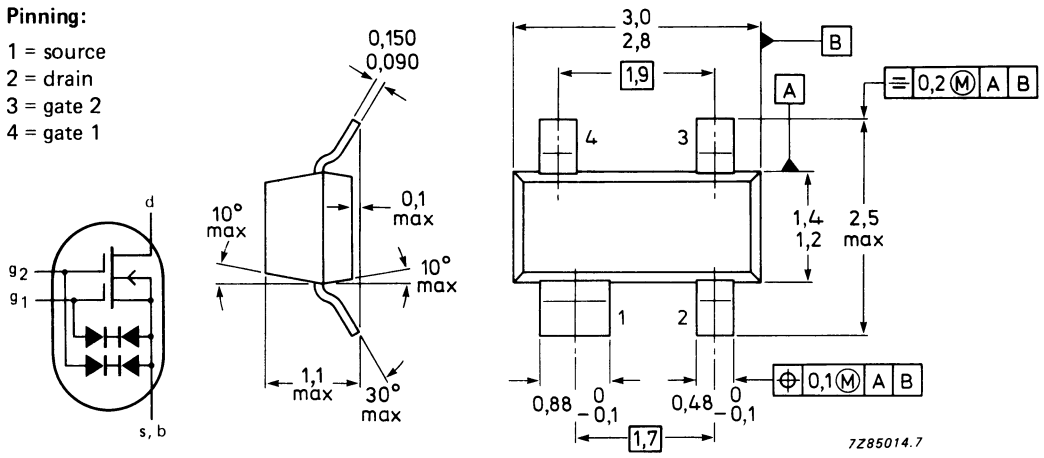
Dimensions in mm

Marking code:

BF989 = MA

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

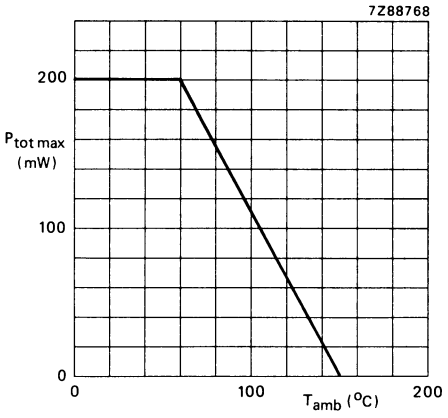


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	max.	50 nA
Drain current			
V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2 to 20 mA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners with 12 V supply voltage and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ. max.	2.0 dB 3.0 dB

MECHANICAL DATA

Fig.1 SOT143.

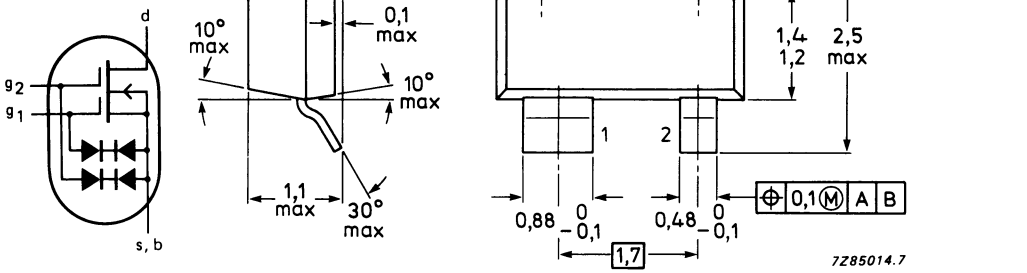
Marking code

BF990A = M86

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

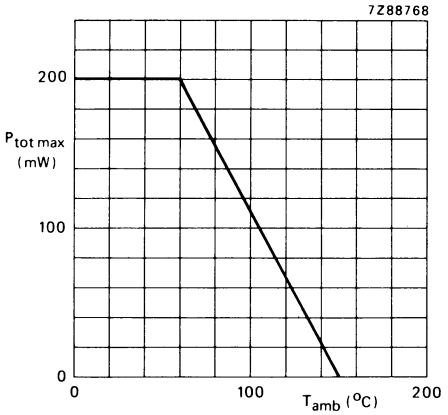


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
gate 1;				
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25	nA
gate 2;				
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25	nA
Gate-source breakdown voltages				
gate 1;				
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20	V
gate 2;				
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20	V
Gate-source cut-off voltages				
gate 1;				
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	1.3	V
gate 2;				
I_D = 20 μA; V_{DS} = 10 V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	max.	1.1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 19	mS mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 3.0	pF pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.4	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2	pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ. max.	2.0 3.0	dB dB

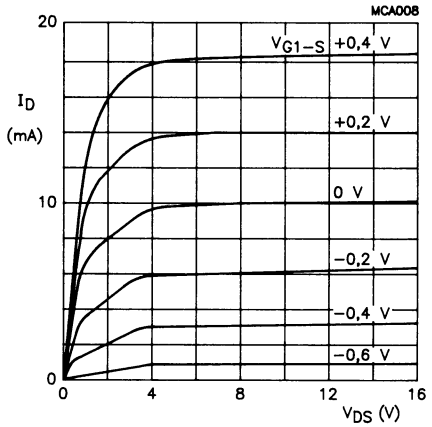


Fig.3 Output characteristics.
V_{G2-S} = 4 V; T_{amb} = 25 °C.

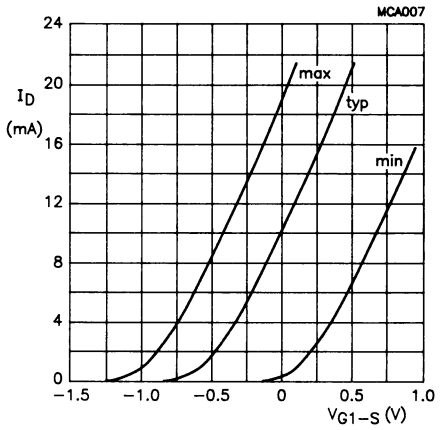


Fig.4 Transfer characteristics.
V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; 3 $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0 dB

MECHANICAL DATA

Fig.1 SOT143R.

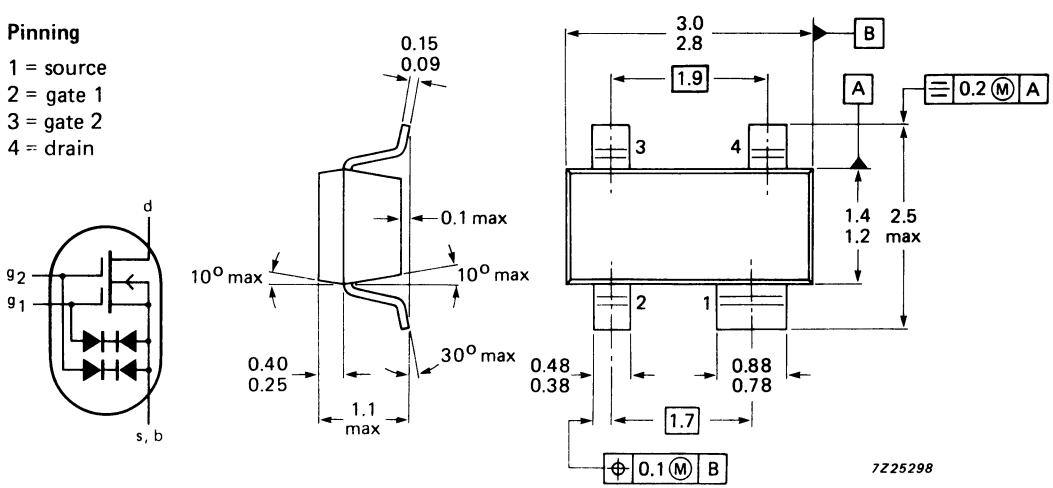
Marking code

BF990AR = M50

Dimensions in mm

Pinning

1 = source
2 = gate 1
3 = gate 2
4 = drain



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
gate 2; $\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	min.	8 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	min.	8 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	1.3 V
gate 2; I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ.	2.0 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,1	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Fig.1 SOT143.

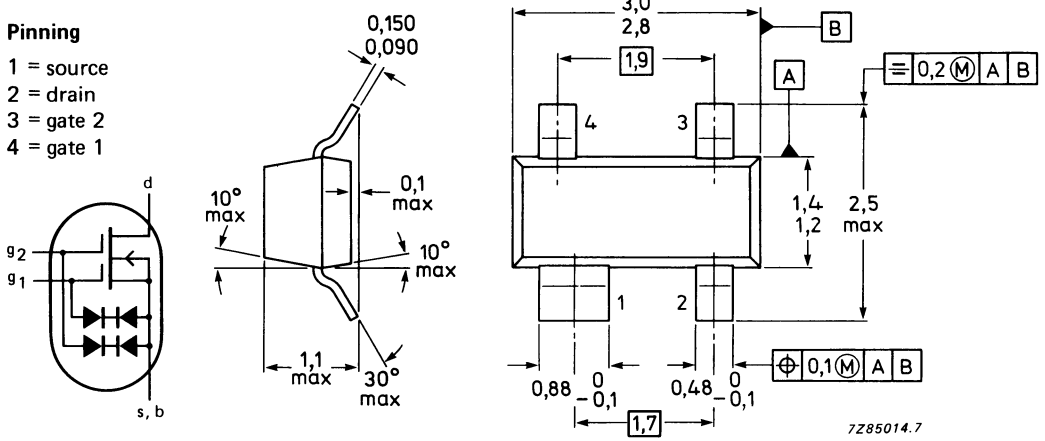
Dimensions in mm

Marking code

BF991 = M91

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

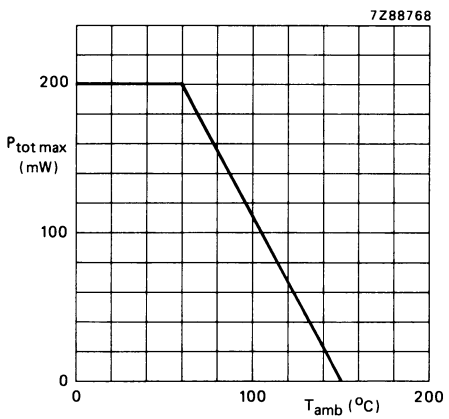


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	<	50	nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	<	50	nA
Drain current				
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		4 to 25	mA
Gate-source breakdown voltages				
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20	V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20	V
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	<	2,5	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	2,5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	10	mS
		typ.	14	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1	pF
Noise figure				
f = 100 MHz; G_S = 1 mS; B_S = B_S opt	F	typ.	0,7	dB
		<	1,7	dB
f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1,0	dB
		<	2,0	dB
Transducer gain (note 1)				
f = 100 MHz; G_S = 1 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	29	dB
f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	26	dB

Note

1. Crystal mounted in a SOT103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

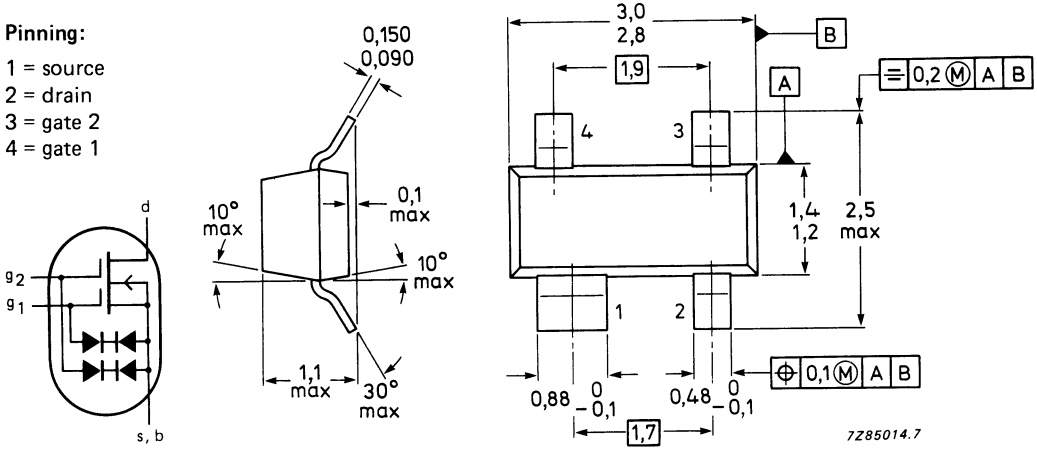
Dimensions in mm

Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

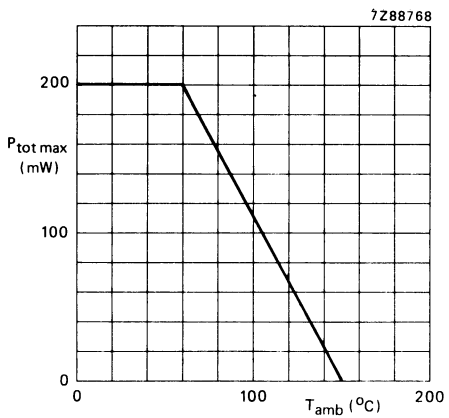


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	max.	25 nA
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		8 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. max.	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

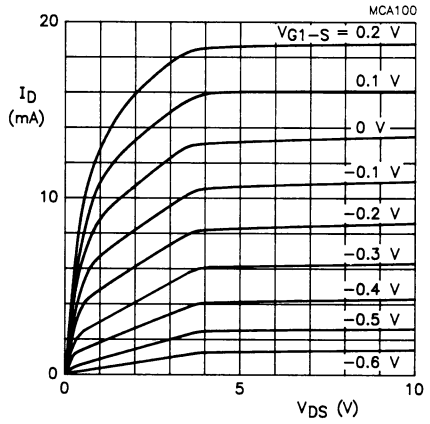


Fig.2 Output characteristics.

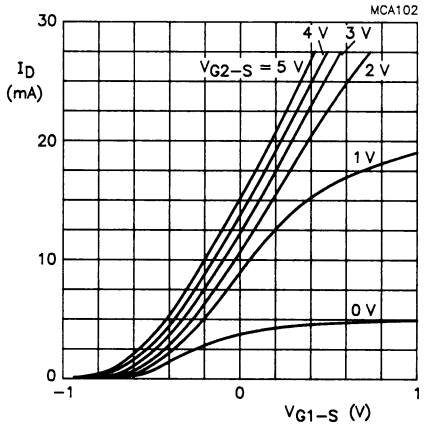


Fig.3 Transfer characteristics.

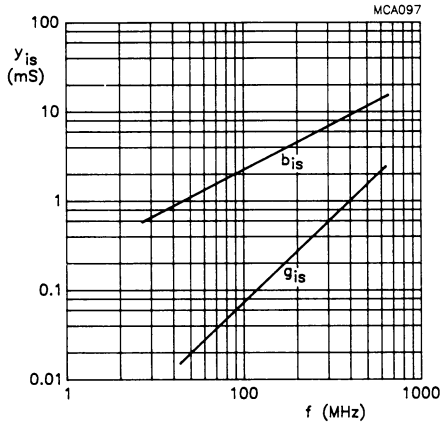


Fig.4 Input admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

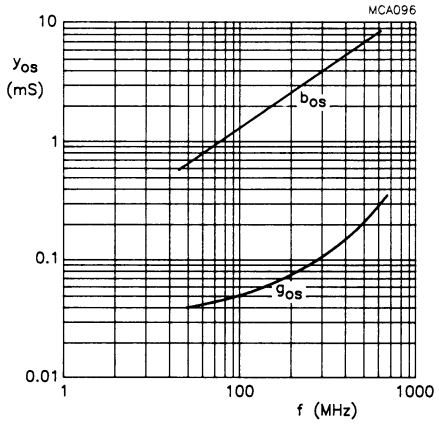


Fig.5 Output admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

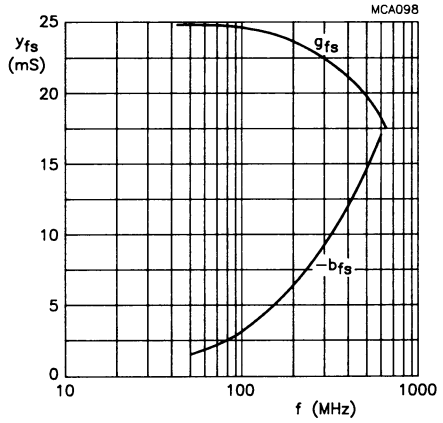


Fig.6 Transfer admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

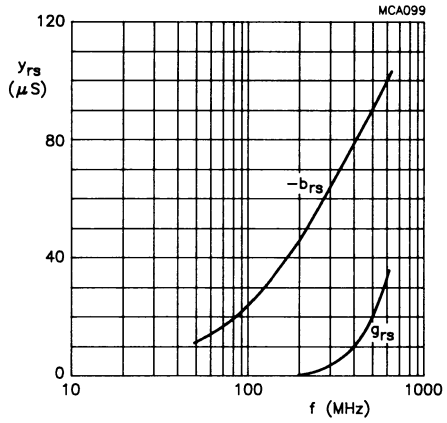


Fig.7 Feedback admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

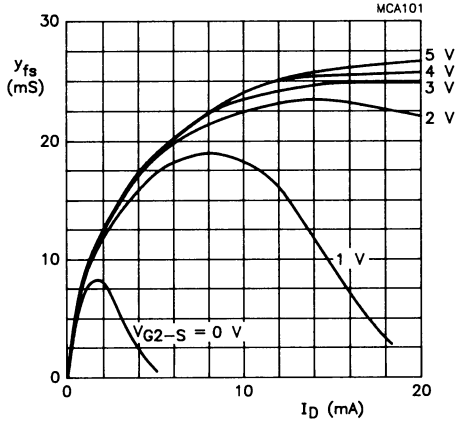


Fig.8 Transfer admittance as a function of drain current.

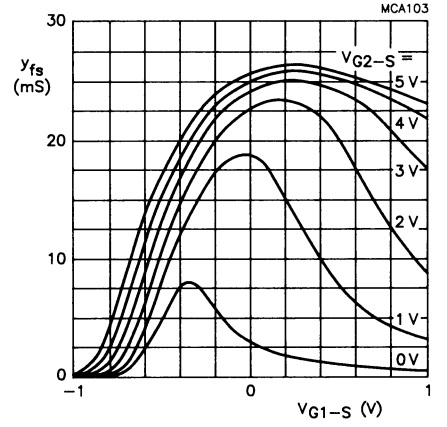


Fig.9 Transfer admittance as a function of gate 2 source voltage.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in VHF applications, such as VHF television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mS
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2	dB

MECHANICAL DATA

Dimensions in mm

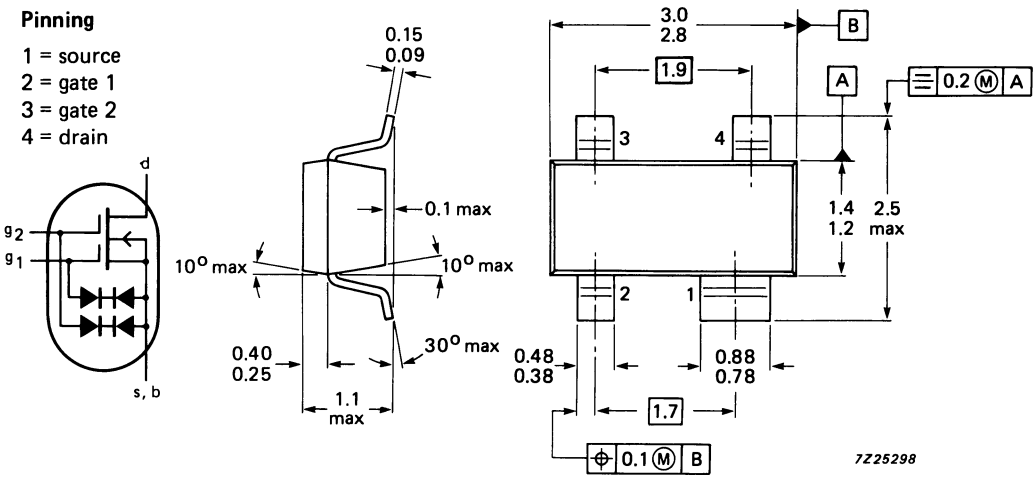
Fig.1 SOT143R.

Marking code

BF992R = M52

Pinning

1 = source
2 = gate 1
3 = gate 2
4 = drain



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. max.	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

MECHANICAL DATA

Dimensions in mm

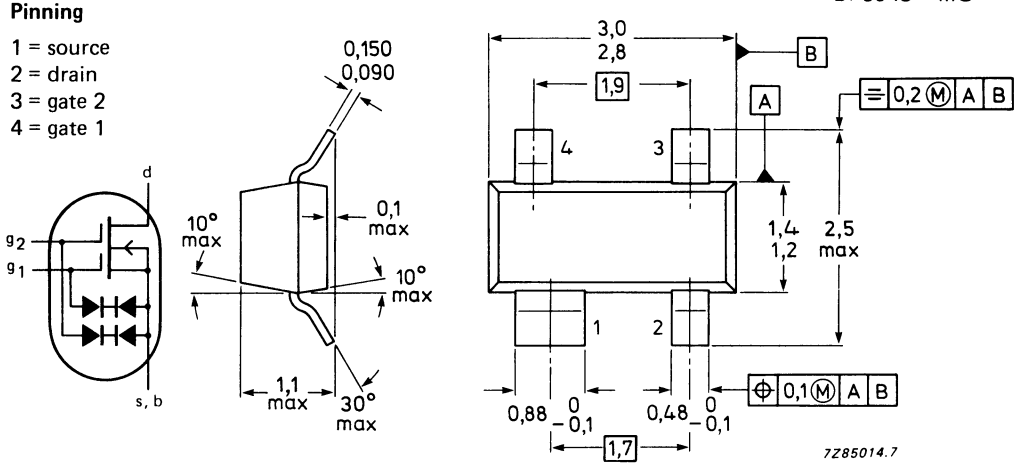
Fig.1 SOT143.

Marking code

BF994S = MG

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
→ Drain current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
→ Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

→ From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

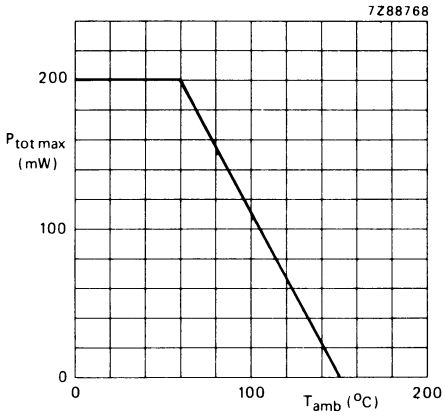


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	50	nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	50	nA
Gate-source breakdown voltages				
± I_{G1-S} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20	V
± I_{G2-S} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20	V
Drain current				
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5	V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15	mS
		typ.	18	mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.5	pF
		max.	3.0	pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0	pF
Noise figure at G_S = 2 mS; B_S = B_S opt; f = 200 MHz	F	typ.	1.0	dB
Power gain at G_S = 2 mS; B_S = B_S opt				
G_L = 0.5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	25	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1: f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4V	C_{ig1-s}	typ. max.	2.5 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Dimensions in mm

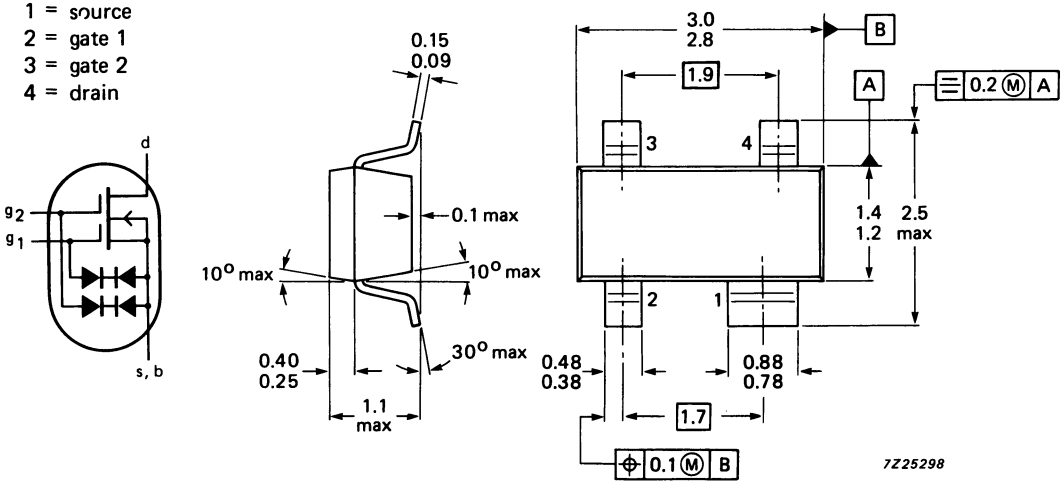
Fig.1 SOT143R.

Pinning

1 = source
2 = gate 1
3 = gate 2
4 = drain

Marking code

BF994SR = M53



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-S}$	max.	50	nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-S}$	max.	50	nA
Gate-source breakdown voltages				
$\pm I_{G1-S}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20	V
$\pm I_{G2-S}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20	V
Drain current				
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5	V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15	mS
		typ.	18	mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.5	pF
		max.	3.0	pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0	pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt; f = 200 MHz	F	typ.	1.0	dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25	dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates ans source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18	mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 2.6	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.8	dB

MECHANICAL DATA

Dimensions in mm

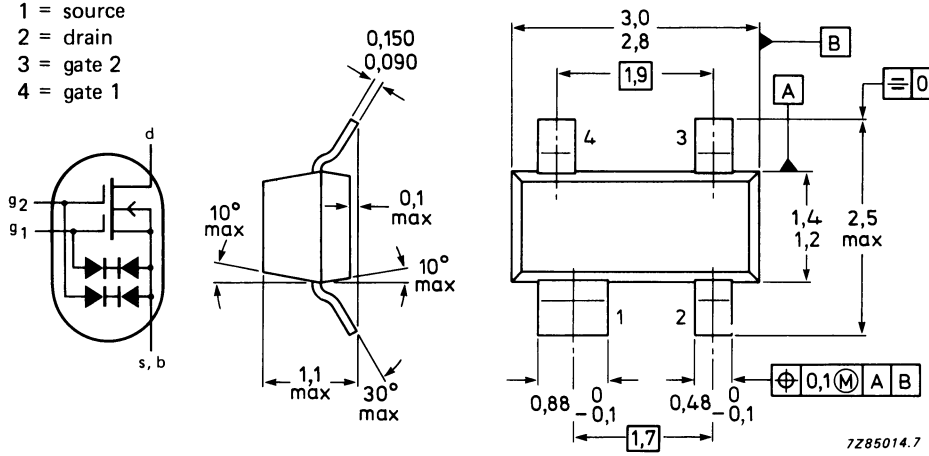
Fig.1 SOT143.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1

Marking code

BF996S = MW



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
→ Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

→ From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

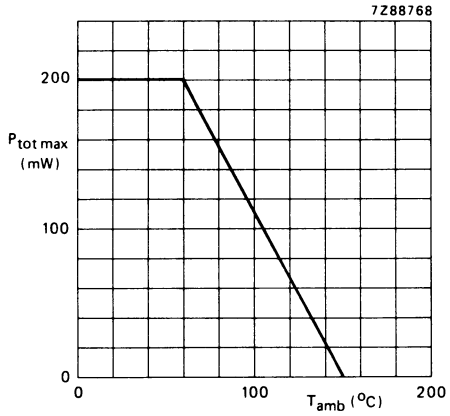


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	50	nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	50	nA
Gate-source breakdown voltages				
± I_{G1-S} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20	V
± I_{G2-S} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20	V
Drain current				
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5	V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15	mS
		typ.	18	mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.3	pF
		max.	2.6	pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8	pF
Noise figure				
f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1.0	dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt		typ.	1.8	dB
Power gain				
f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0.5 mS; B_L = B_L opt	G_p	typ.	25	dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt; G_L = 1.0 mS; B_L = B_L opt		typ.	18	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.8 dB

MECHANICAL DATA

Dimensions in mm

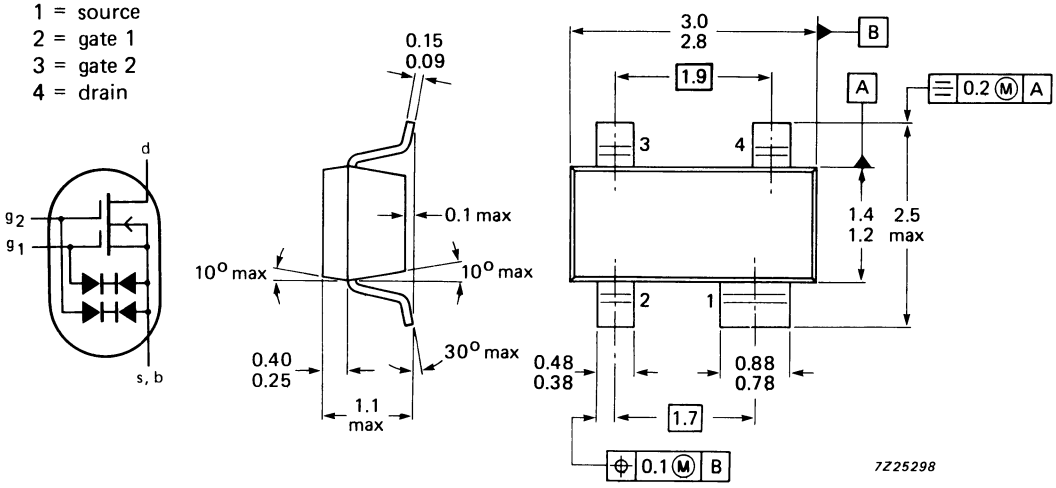
Fig.1 SOT143R.

Marking code

BF996SR = M95

Pinning

1 = source
2 = gate 1
3 = gate 2
4 = drain



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	50	nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	50	nA
Gate-source breakdwon voltages				
$\pm I_{G1-S}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20	V
$\pm I_{G2-S}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20	V
Drain current				
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20	mA
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5	V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15	mS
		typ.	18	mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.3	pF
		max.	2.6	pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8	pF
Noise figure				
f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0	dB
f = 800 MHz; G_S = 3.3 mS; $B_S = B_S$ opt		typ.	1.8	dB
Power gain				
f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt; G_L = 0.5 mS; $B_L = B_L$ opt	G_p	typ.	25	dB
f = 800 MHz; G_S = 3.3 mS; $B_S = B_S$ opt; G_L = 1.0 mS; $B_L = B_L$ opt		typ.	18	dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

QUICK REFERENCE DATA

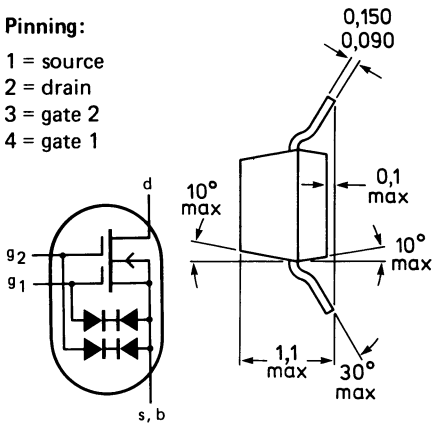
Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2.5	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

MECHANICAL DATA

Fig.1 SOT143.

Pinning:

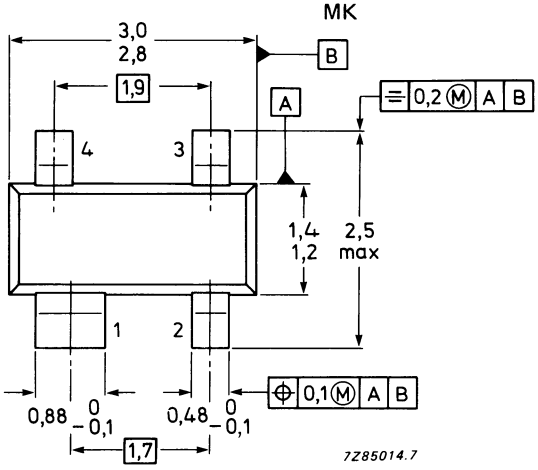
1 = source
2 = drain
3 = gate 2
4 = gate 1



Dimensions in mm

Marking code:

MK



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
→ Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

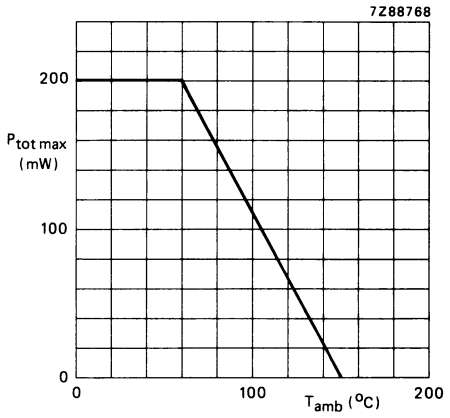


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
gate 2; $\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
gate 2; I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V
Drain-source cut-off voltage V_{DS} = 15 V; V_{G2-S} = 4 V; V_{G1-S} = 0	I_{DSS}		2 to 20 mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.5 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a metal TO-72 envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:
a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
b) excellent signal handling capability over the entire gain control range.
c) low noise figure combined with high gain.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	175	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	15	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	5.5	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V G_S = 1.2 mA; $-B_S$ = 5.7 mS; f = 200 MHz	F	typ.	2.3	dB

MECHANICAL DATA

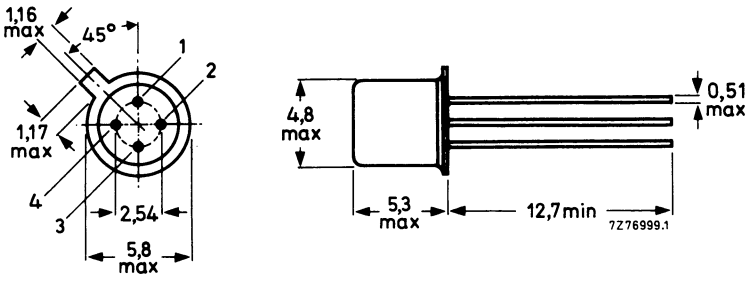
Dimensions in mm

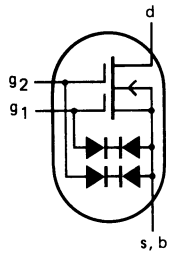
Fig.1 TO-72.

Source and substrate connected to the case.

Pinning:

1 = drain
2 = gate 2
3 = gate 1
4 = source





Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$

Gate cut-off currents			
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	10 nA
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$; $T_j = 150\ ^oC$	$\pm I_{G1-SS}$	max.	10 μA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	10 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$; $T_j = 150\ ^oC$	$\pm I_{G2-SS}$	max.	10 μA
Gate-source breakdown voltages			
$\pm I_{G1-SS} = 0.1$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS} = 0.1$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
$V_{DS} = 10$ V; $V_{G1-S} = 0$; + $V_{G2-S} = 4$ V	I_{DSS}		20 to 55 mA
Gate 1-source voltage			
$I_D = 10$ mA; $V_{DS} = 10$ V; + $V_{G2-S} = 4$ V	$-V_{G1-SS}$		0.6 to 2.1 V
Gate-source cut-off voltages			
$I_D = 10$ μA; $V_{DS} = 10$ V; + $V_{G2-S} = 4$ V	$-V_{(P)G1-S}$		1.5 to 3.8 V
$I_D = 10$ μA; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$		1.5 to 3.4 V

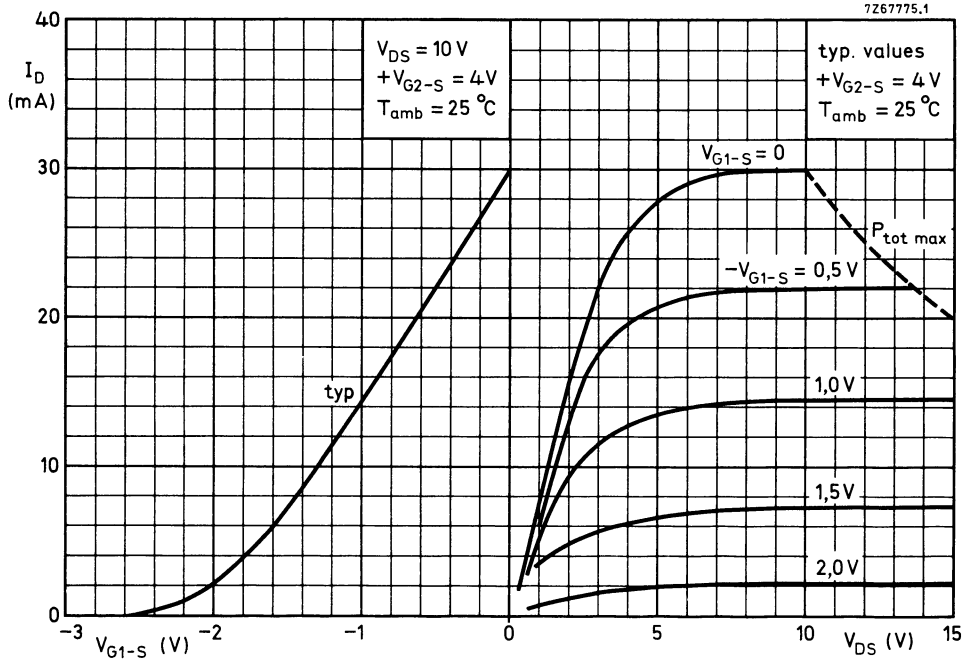
DYNAMIC CHARACTERISTICS

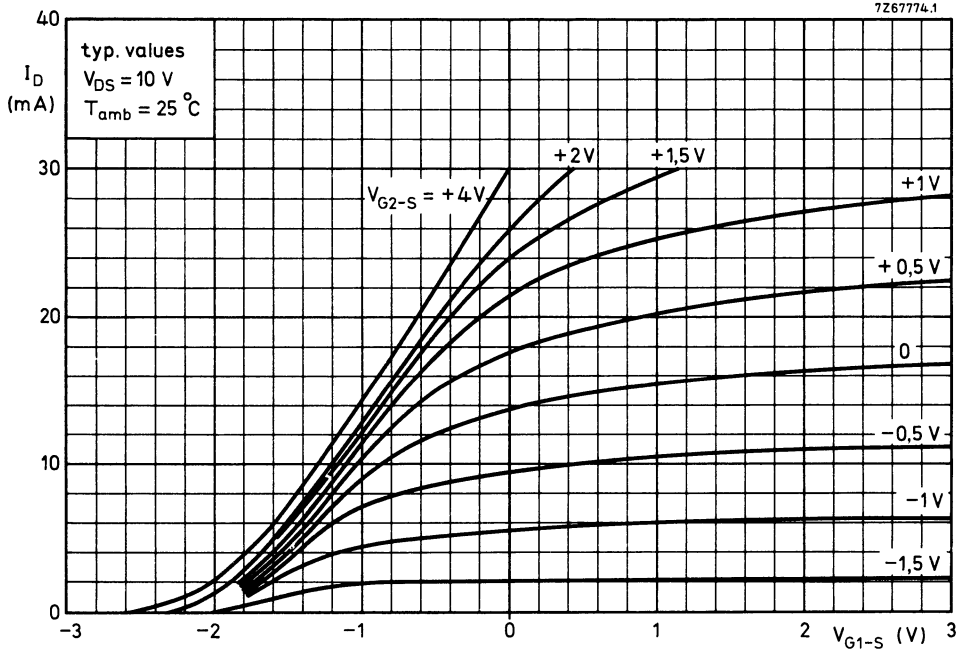
Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; + $V_{G2-S} = 4$ V; $T_{amb} = 25\ ^oC$

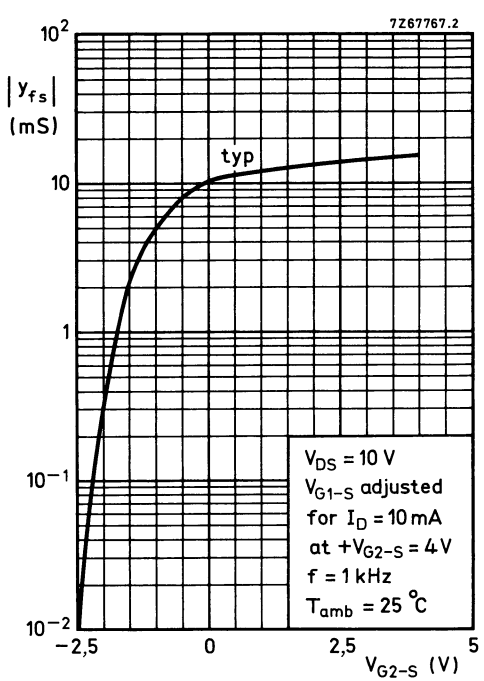
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	12 mS
		typ.	15 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	5.5 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3.5 pF
Noise figure at optimum source admittance			
$G_S = 0.95$ mS; $-B_S = 5.0$ mS; f = 100 MHz	F	typ.	1.9 dB
$G_S = 1.20$ mS; $-B_S = 5.7$ mS; f = 200 MHz	F	typ.	2.3 dB
		max.	3.0 dB
Cross modulation at f = 200 MHz			
Wanted signal at $f_o = 197.5$ MHz			
Unwanted signal at $f_{int} = 202.5$ MHz			
Interference voltage at g_1 for K = 1%	V_{int}	typ.	100 mV (note 1)

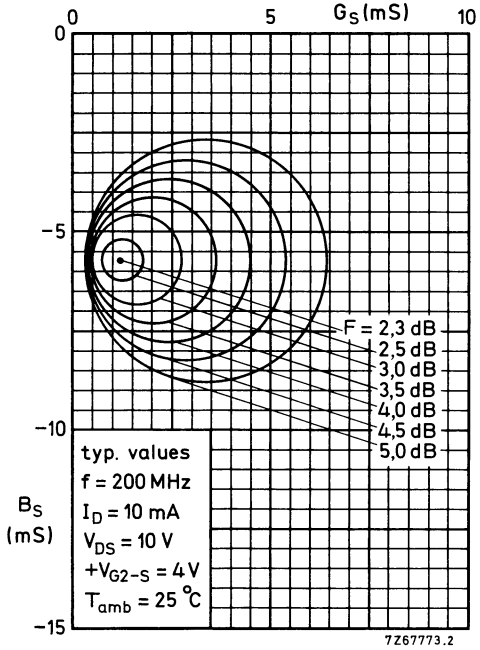
Note

1. Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0.8% modulation depth on the wanted signal (a.m. definition).


7Z67775.1
I_D (mA)
V_{DS} = 10 V
+V_{G2-S} = 4 V
T_{amb} = 25 °C
typ. values
+V_{G2-S} = 4 V
T_{amb} = 25 °C
V_{G1-S} = 0
$P_{tot\ max}$
−V_{G1-S} = 0,5 V
1,0 V
1,5 V
2,0 V
typ
V_{G1-S} (V)
V_{DS} (V)


7Z67774.1
I_D (mA)
typ. values
V_{DS} = 10 V
T_{amb} = 25 °C
+2 V
+1,5 V
V_{G2-S} = +4 V
+1 V
+0,5 V
0
−0,5 V
−1 V
−1,5 V
V_{G1-S} (V)





circles of constant noise figure

DEVICE DATA
VERTICAL D-MOS-FETs

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as line current interruptor in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC)	I_D	max.	120 mA
Total power dissipation up to T_c = 25 °C	P_{tot}	max.	500 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 2.6 V; I_D = 20 mA	R_{DSon}	max.	28 Ω

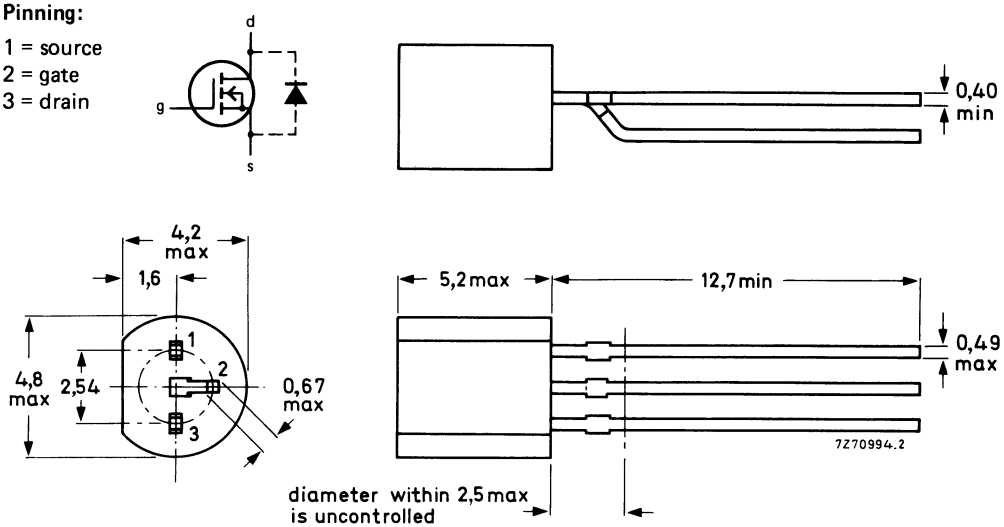
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DSS}	max.	200	V
Drain-gate voltage	V_{DGS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15	V
Drain current (DC)	I_D	max.	120	mA
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.	500	mW
Storage temperature range	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0$; $I_D = 100\ \mu A$	$V_{(BR)DSS}$	min.	200	V
Gate-source leakage current $V_{GS} = 15$ V; $V_{DS} = 0$	I_{GSoff}	max.	10	nA
Drain cut-off current				
$V_{DS} = 130$ V; $V_{GS} = 0$	I_{DSS}	max.	30	nA
$V_{DS} = 70$ V; $V_{GS} = 0.2$ V	I_{DSX}	max.	1	μA
Drain-source ON-resistance				
$V_{GS} = 2.6$ V; $I_D = 20$ mA	R_{DSon}	typ.	15	Ω
		max.	28	Ω
$V_{GS} = 10$ V; $I_D = 250$ mA	R_{DSon}	typ.	6	Ω
Gate threshold voltage		min.	0.8	V
$I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	typ.	1.8	V
		max.	2.8	V
Transfer admittance $I_D = 250$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{iss}	typ.	70	pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{oss}	typ.	20	pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rss}	typ.	5	pF
Switching times (see Figs 2 and 3)				
$I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

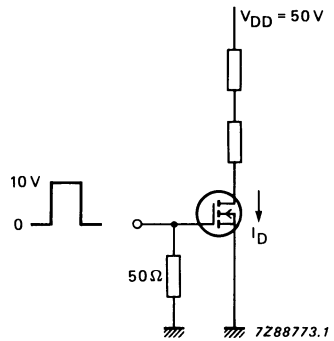


Fig. 2 Switching times test circuit.

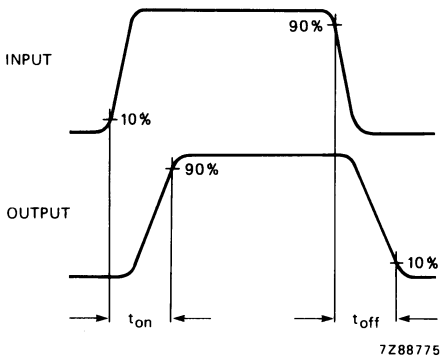


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	200 mS 350 mS

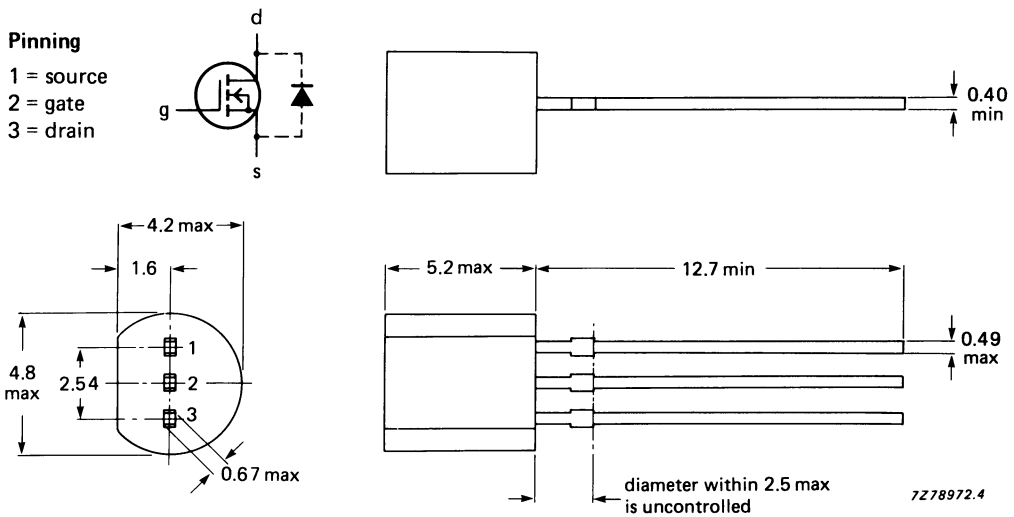
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinnings are available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Storage temperature	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 130 V; V_{GS} = 0	I_{DSS}	max.	30 nA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.0 V 3.0 V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.2 Ω 6.0 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

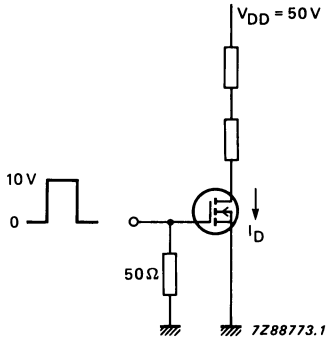


Fig.2 Switching times test circuit.

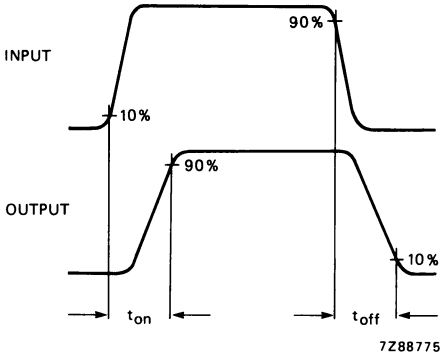


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5 Ω

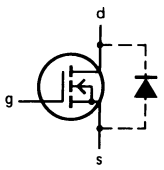
MECHANICAL DATA

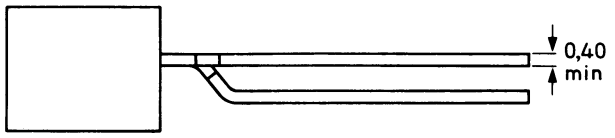
Dimensions in mm

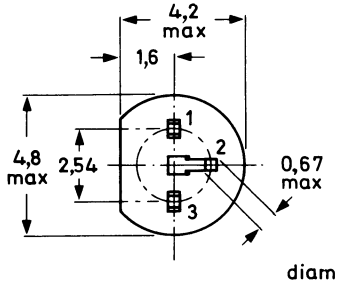
Fig. 1 TO-92 variant.

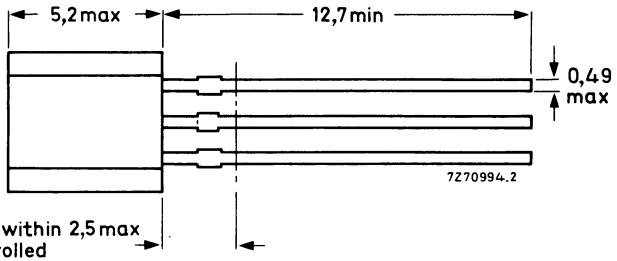
Pinning:

1 = source
2 = gate
3 = drain









Note: Various pin configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC) at T_c = 25 °C	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
V_{GS} = 0; I_D = 100 μA	$V_{(BR)DSS}$	min.	60 V
		typ.	90 V
Gate threshold voltage			
V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min.	0.8 V
		max.	3.0 V
Gate-source leakage current			
V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10 nA
Drain cut-off current			
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5 μA
Drain-source ON-resistance			
V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	typ.	2.5 Ω
		max.	5.0 Ω
Transfer admittance			
V_{DS} = 10 V; I_D = 200 mA;	$\lvert Y_{fs} \rvert$	typ.	200 mS
Capacitances at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	25 pF
		max.	40 pF
	C_{oss}	typ.	22 pF
		max.	30 pF
	C_{rss}	typ.	6 pF
		max.	10 pF
Switching times at I_D = 200 mA			
I_D = 200 mA; V_{DD} = 50 V;	t_{on}	typ.	4 ns
		max.	10 ns
V_{GS} = 0 to 10 V	t_{off}	typ.	4 ns
		max.	10 ns

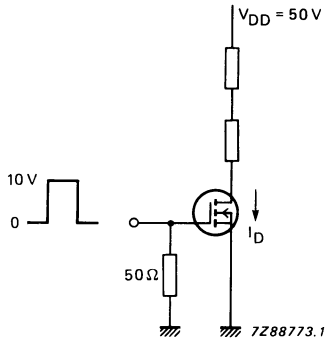


Fig. 2 Switching times test circuit.

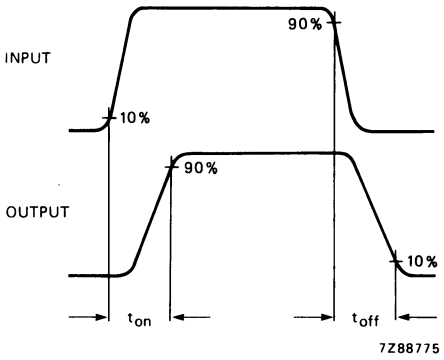


Fig. 3 Input and output waveforms.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

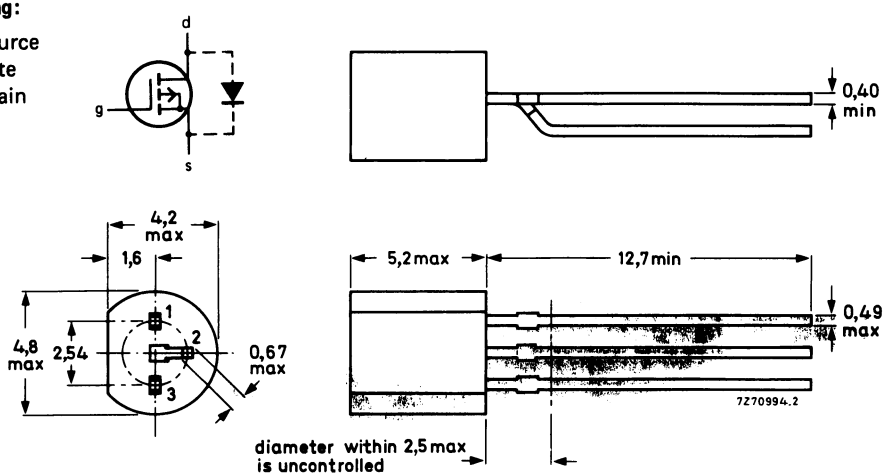
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak value)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	45 V
Drain-source leakage current $-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5 μA
Gate-source leakage current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.0 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

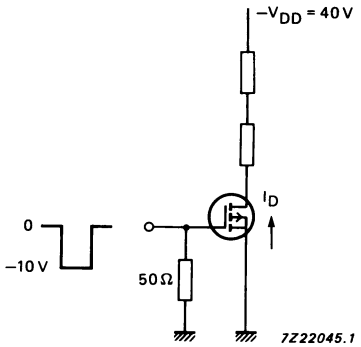


Fig. 2 Switching times test circuit.

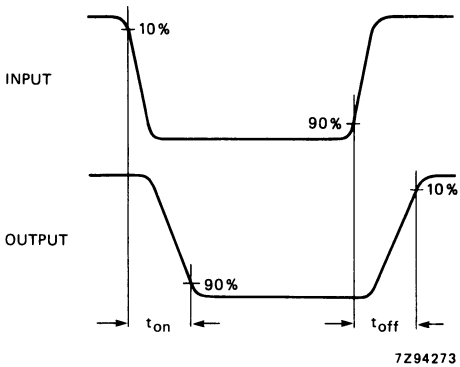


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS

MECHANICAL DATA

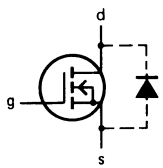
Dimensions in mm

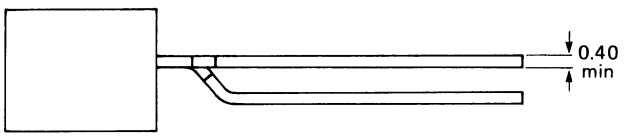
Fig.1 TO-92 variant.

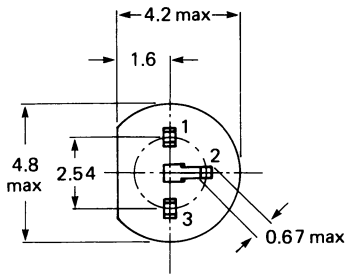
Pinning

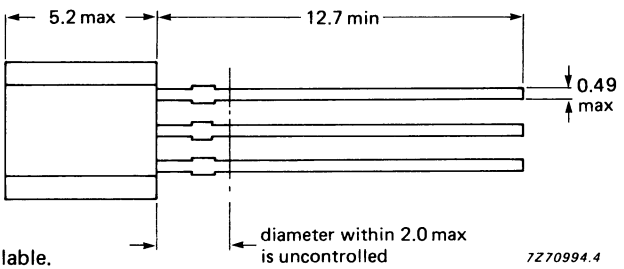
BSN205
1 = gate
2 = drain
3 = source

BSN205A
1 = source
2 = gate
3 = drain









Note: various pinout configurations available.

7Z70994.4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	3.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

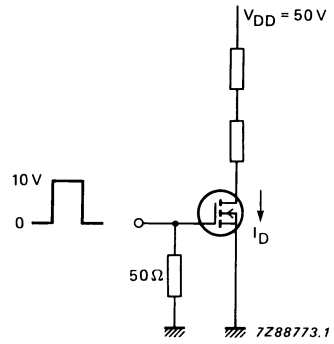


Fig.2 Switching time test circuit.

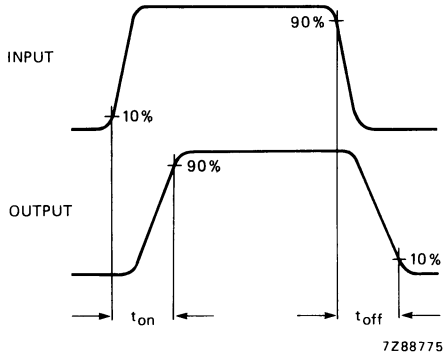


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 400 mS

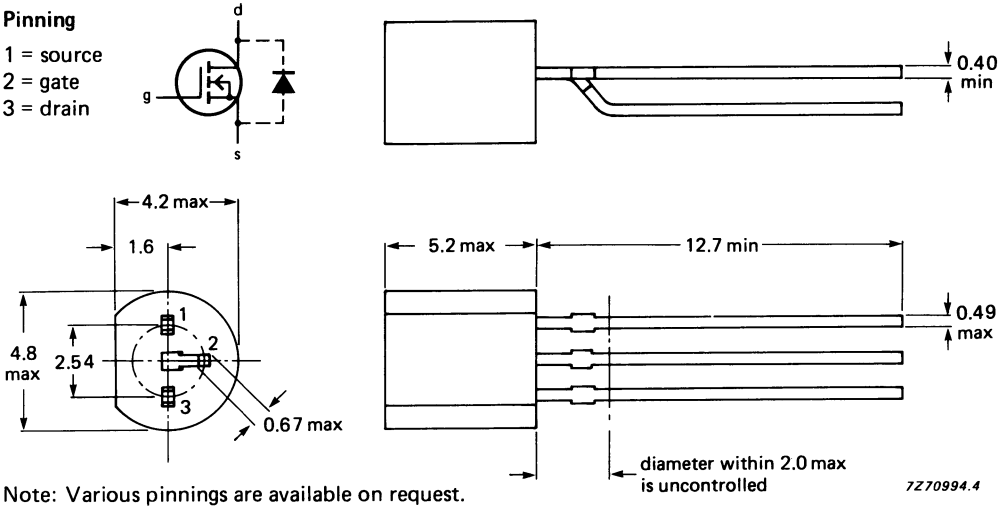
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250 V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.0 V
Drain-source ON-resistance I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
I_D = 20mA; V_{GS} = 2.4V	R_{DSon}	max.	10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 400 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 15 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	20 ns 30 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

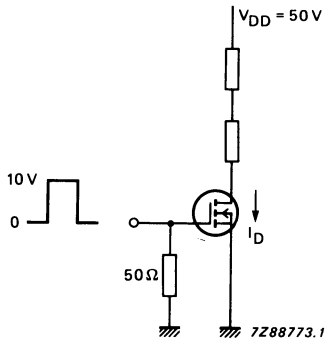


Fig.2 Switching times test circuit.

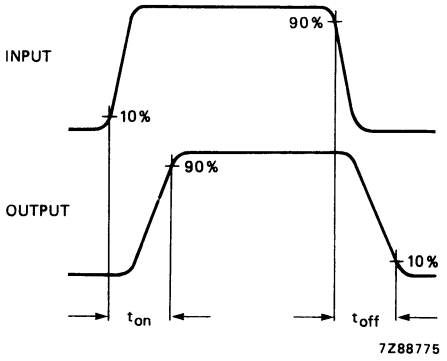


Fig.3 Input and output waveforms.

DEVELOPMENT DATA

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 15 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS

MECHANICAL DATA

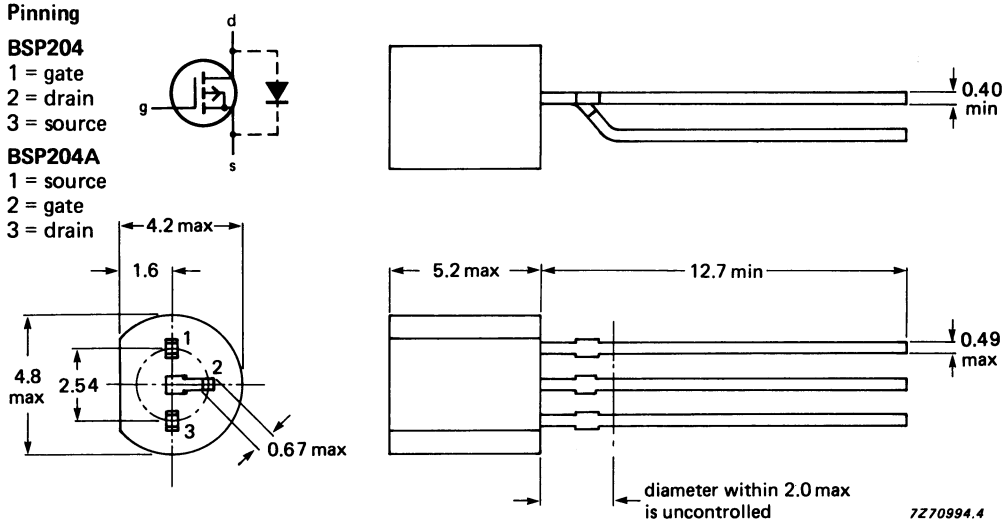
Dimensions in mm

Fig.1 TO-92 variant.

Pinning

BSP204
1 = gate
2 = drain
3 = source

BSP204A
1 = source
2 = gate
3 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.6 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	200 V
Drain-source leakage current $-V_{DS}$ = 160 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 15 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{iss}	typ. max.	65 pF 90 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{rss}	typ. max.	6 pF 15 pF
Switching times (see Figs 2 and 3) $-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	20 ns 30 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

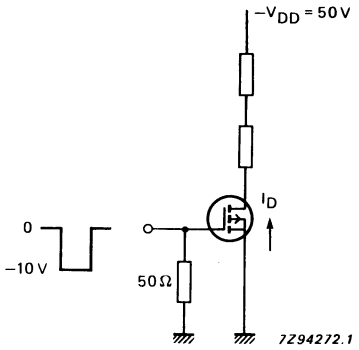


Fig. 2 Switching time test circuit.

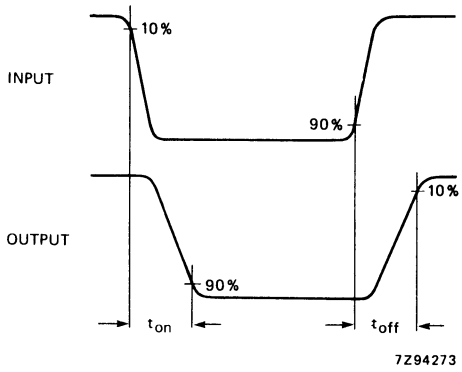


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in a SOT89 envelope.
Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	max. typ.	6 Ω 4.5 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ. min.	350 mS 140 mS

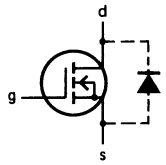
MECHANICAL DATA

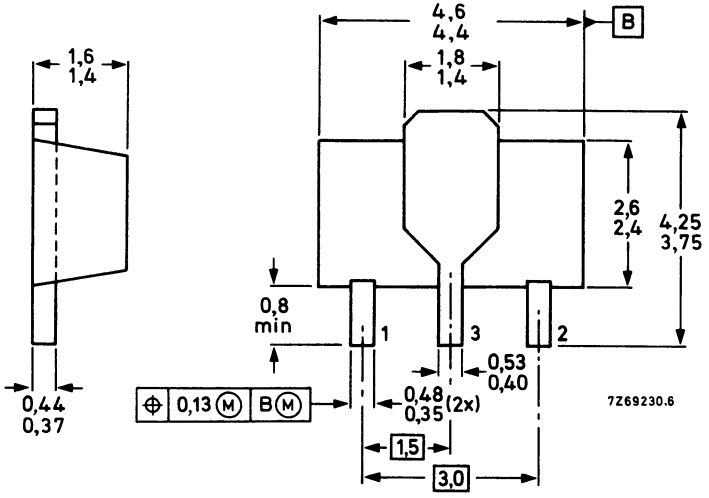
Dimensions in mm

Fig. 1 SOT89.

Pinning

1 = source
2 = gate
3 = drain





marking: KA

BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Drain current (peak)	I_{DM}	max.	1.1 A
Total power dissipation up to T_{amb} = 25 °C *	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient *	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0 V_{DS} = 200 V; V_{GS} = 0	I_{DSS} I_{DSS}	max. max. typ.	200 nA 60 μA 100 nA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max. typ.	6 Ω 4.5 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ. min.	350 mS 140 mS
Input capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max. typ.	60 pF 45 pF
Output capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max. typ.	25 pF 15 pF
Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max. typ.	10 pF 3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10	t_{on} t_{off}	typ. max. typ. max.	5 ns 10 ns 15 ns 25 ns

* Transistor mounted on ceramic substrate area 2.5 cm², thickness 0.7 mm.

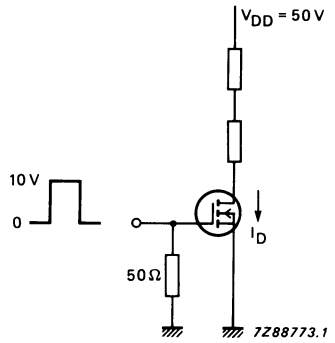


Fig. 2 Switching times test circuit.

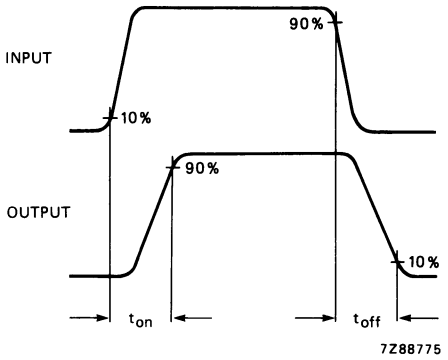


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

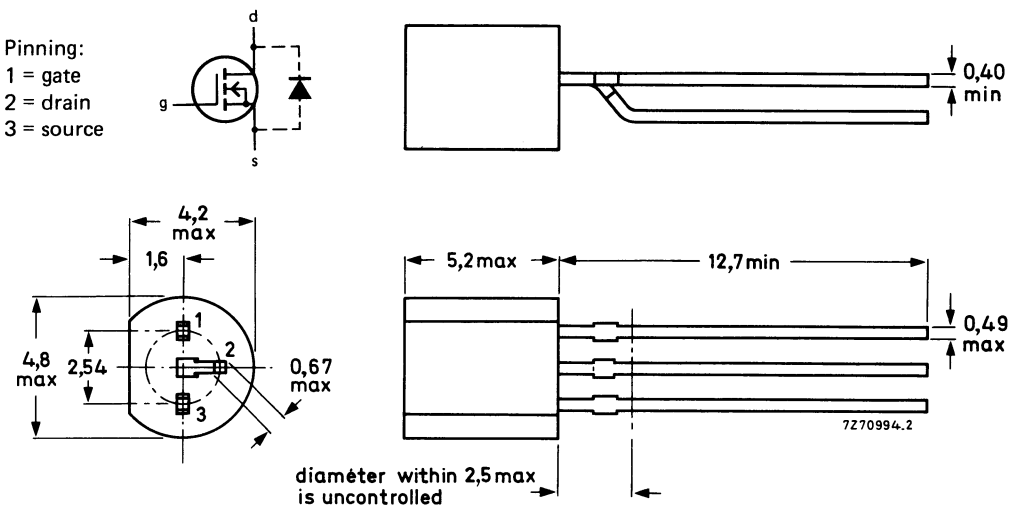
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 mS 350 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−55 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ. max.	100 nA 60 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 15 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

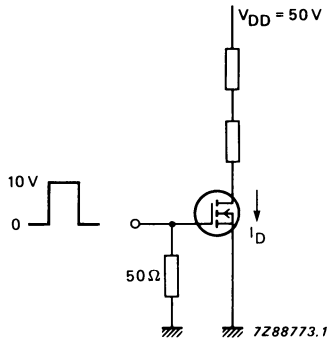


Fig. 2 Switching time test circuit.

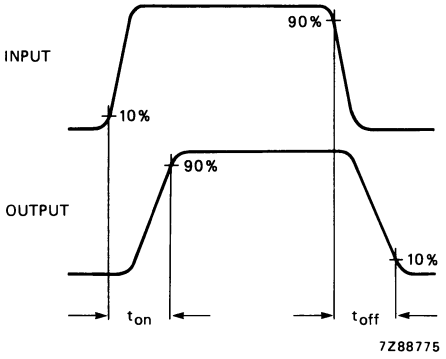


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-18 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.0 Ω	
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	140 mS 350 mS	

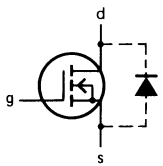
MECHANICAL DATA

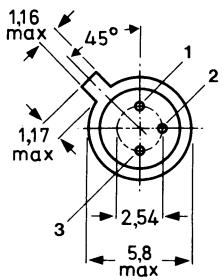
Dimensions in mm

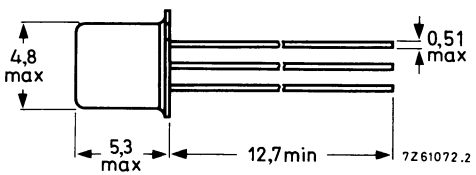
Fig. 1 TO-18.

Pinning

1 = source
2 = gate
3 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.4 A
Total power dissipation up to			
T_{amb} = 25 °C	P_{tot}	max.	0.4 W
T_{case} = 25 °C	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	310 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
→ I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
→ V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ.	100 nA
		max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
→ Gate threshold voltage	$V_{GS(th)}$	min.	0.8 V
I_D = 1 mA; V_{DS} = V_{GS}		max.	2.8 V
Drain-source ON-resistance	R_{DSon}	typ.	4.5 Ω
I_D = 400 mA; V_{GS} = 10 V		max.	6.0 Ω
Transfer admittance	$\lvert y_{fs} \rvert$	min.	140 mS
I_D = 400 mA; V_{DS} = 25 V		typ.	250 mS
Input capacitance at f = 1 MHz;	C_{iss}	typ.	45 pF
V_{DS} = 25 V; V_{GS} = 0		max.	60 pF
Output capacitance at f = 1 MHz;	C_{oss}	typ.	15 pF
V_{DS} = 25 V; V_{GS} = 0		max.	25 pF
Feedback capacitance at f = 1 MHz;	C_{rss}	typ.	3.5 pF
V_{DS} = 25 V; V_{GS} = 0		max.	10 pF
Switching times (see Figs 2 and 3)	t_{on}	typ.	5 ns
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V		max.	15 ns
	t_{off}	typ.	15 ns
		max.	25 ns

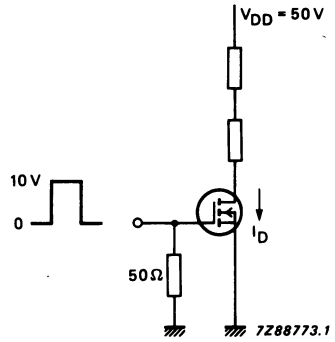


Fig. 2 Switching time test circuit.

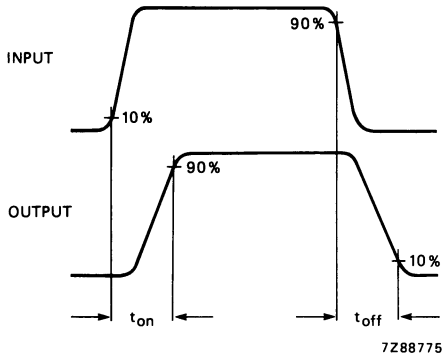


Fig. 3 Input and output waveforms.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

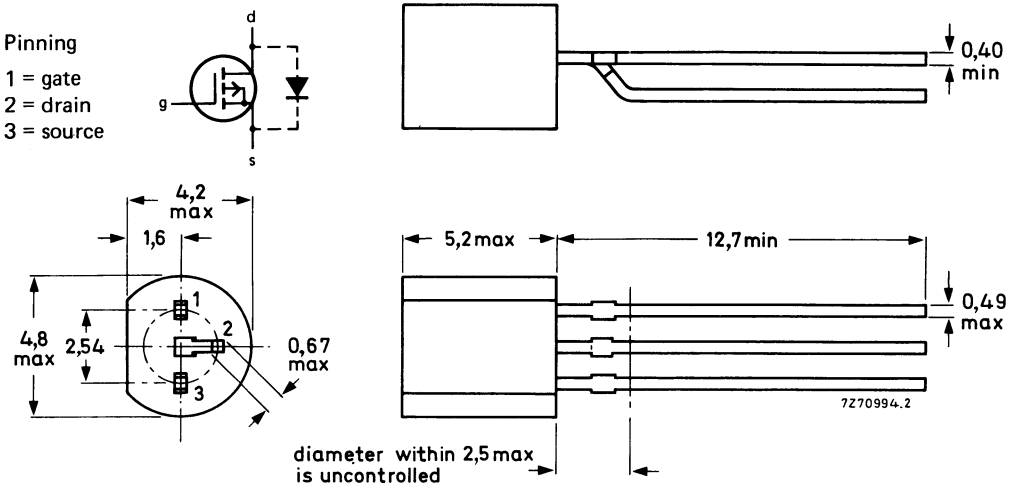
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 mS 200 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Drain current (peak)	$-I_{DM}$	max.	0.6 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
$-I_D$ = 250 μA; $-V_{GS}$ = 0	$-V_{(BR)DS}$	min.	200 V
Drain-source leakage current			
$-V_{DS}$ = 60 V; $-V_{GS}$ = 0	$-I_{DSS}$	max.	0.2 μA
$-V_{DS}$ = 200 V; $-V_{GS}$ = 0	$-I_{DSS}$	max.	60 μA
Gate-source leakage current			
$-V_{GS}$ = 20 V; $-V_{DS}$ = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage			
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	0.8 V
		max.	2.8 V
Drain-source ON-resistance			
$-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ.	10 Ω
		max.	20 Ω
Transfer admittance			
$-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min.	60 mS
		typ.	200 mS
Input capacitance at f = 1 MHz;			
$-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{iss}	typ.	65 pF
Output capacitance at f = 1 MHz;			
$-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{oss}	typ.	20 pF
Feedback capacitance at f = 1 MHz;			
$-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{rss}	typ.	6 pF
Switching times (see Figs 2 and 3)			
$-I_D$ = 250 mA; $-V_{DD}$ = 50 V;	t_{on}	typ.	5 ns
$-V_{GS}$ = 0 to 10 V	t_{off}	typ.	20 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

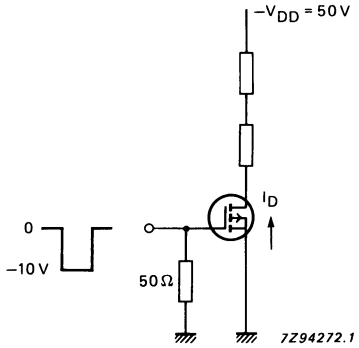


Fig. 2 Switching time test circuit.

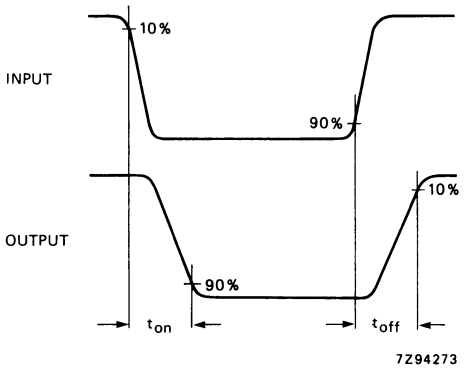


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2 Ω 4 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS

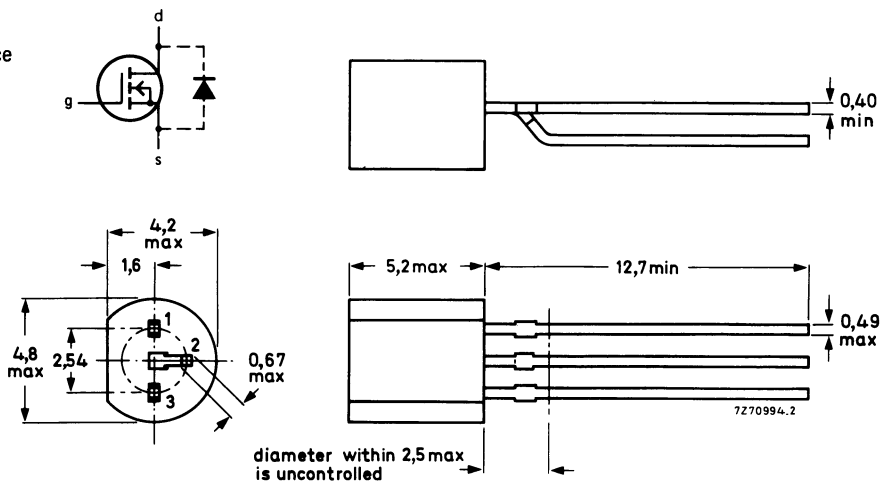
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

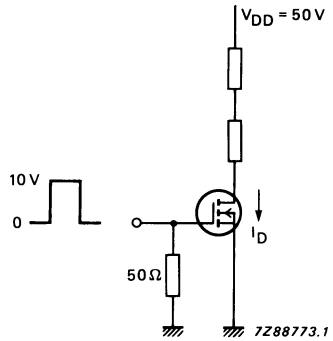


Fig. 2 Switching times test circuit.

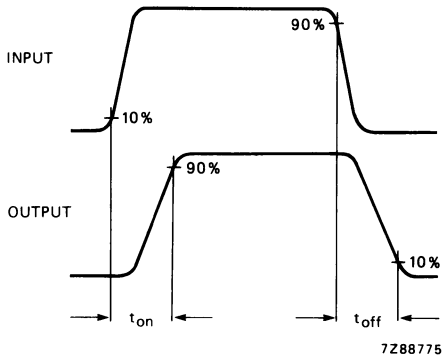


Fig. 3 Input and output waveforms.

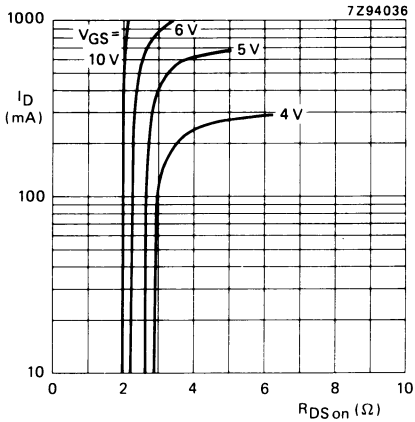


Fig. 4 T_j = 25 °C; typical values.

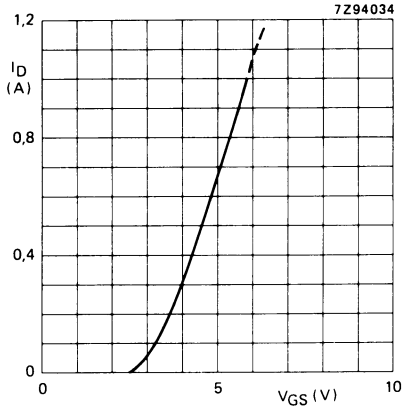


Fig. 5 T_j = 25 °C; typical values at V_{DS} = 10 V.

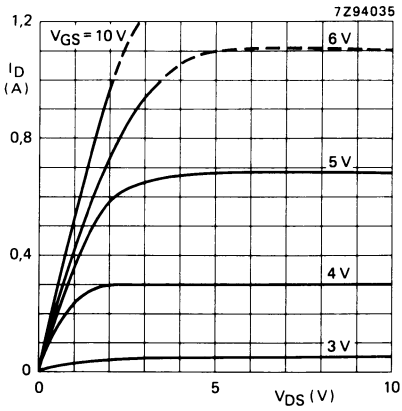


Fig. 6 T_j = 25 °C; typical values.

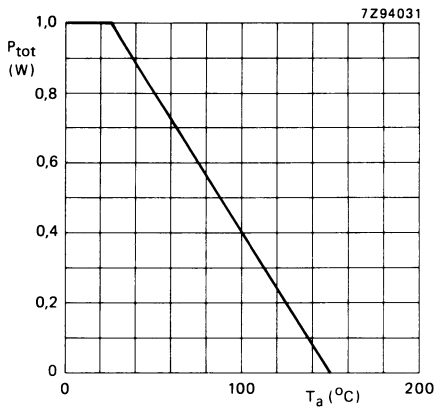


Fig. 7 Power derating curve.

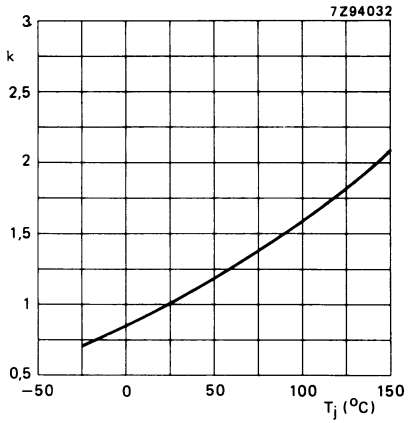


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 500 mA/10 V.

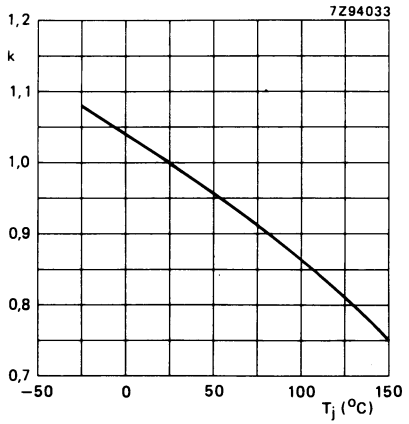


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

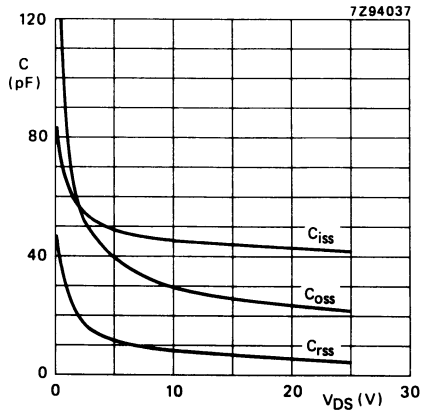


Fig. 10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	0.83 W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V	$\lvert y_{fs} \rvert$	typ.	150 mS

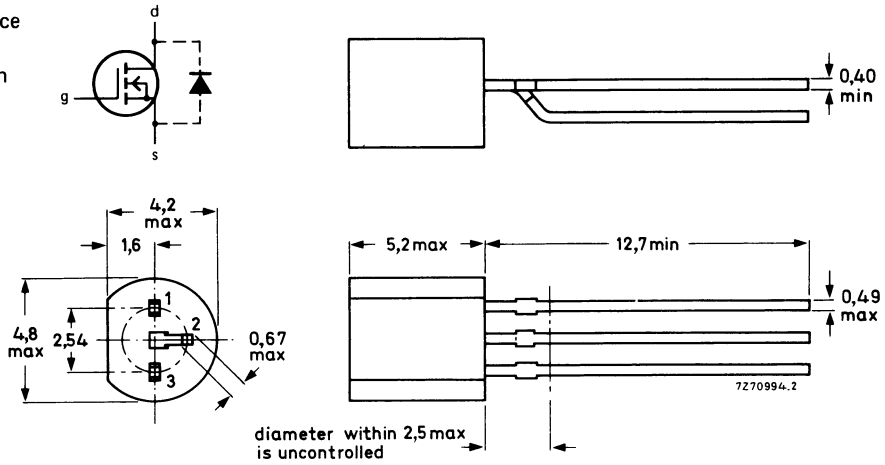
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance (see Fig. 4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 20	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 6	pF pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	4 10	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

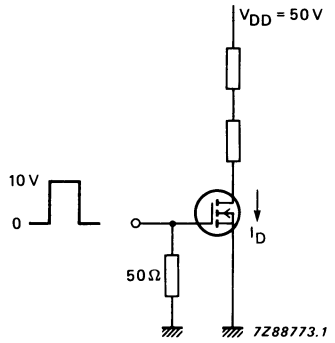


Fig. 2 Switching times test circuit.

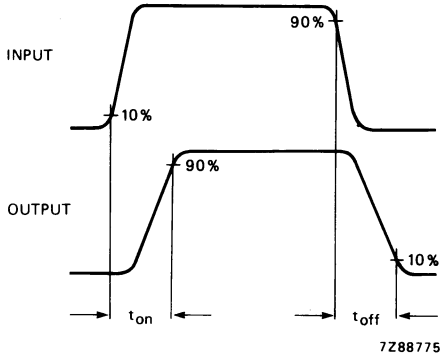


Fig. 3 Input and output waveforms.

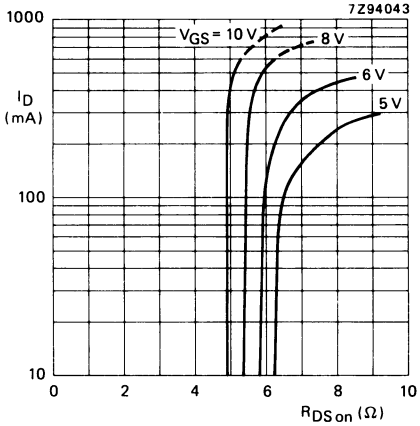


Fig. 4 T_j = 25 °C; typical values.

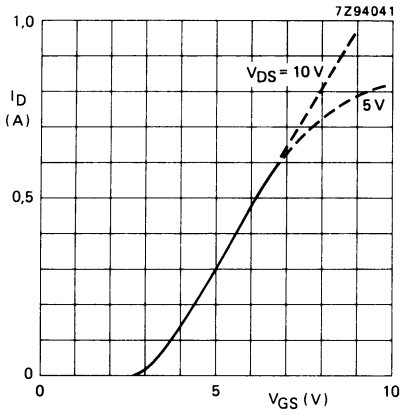


Fig. 5 T_j = 25 °C; typical values.

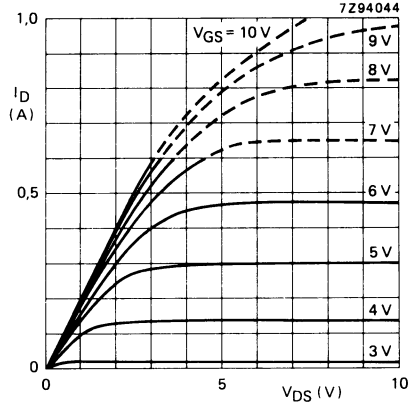


Fig. 6 T_j = 25 °C; typical values.

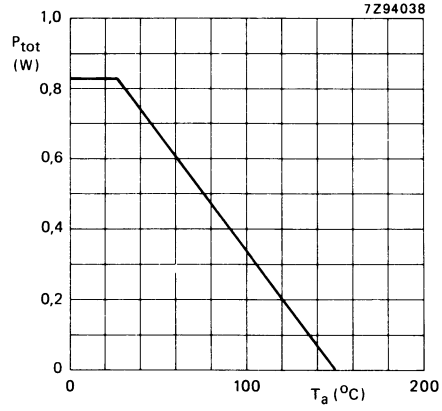


Fig. 7 Power derating curve.

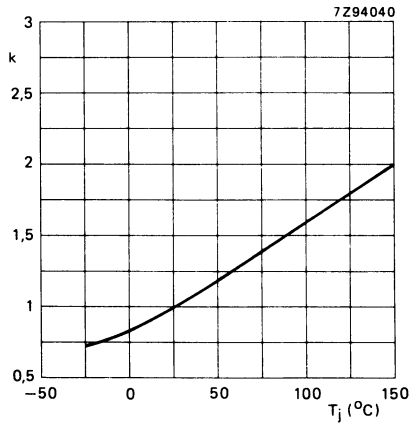


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typ. values at 150 mA/5 V.

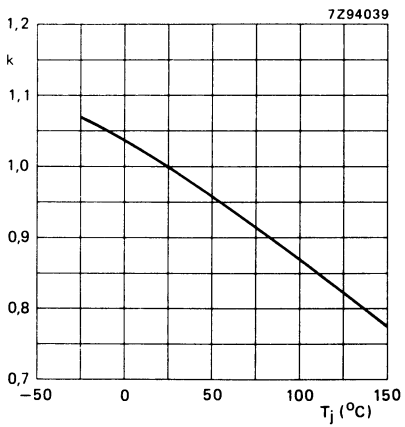


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

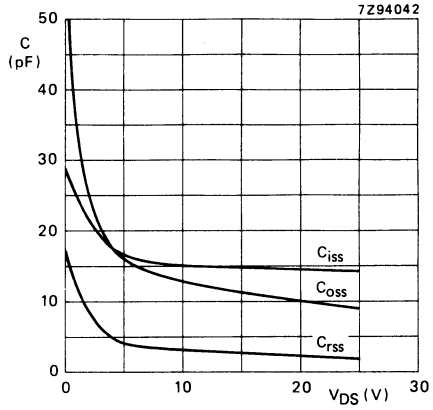


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

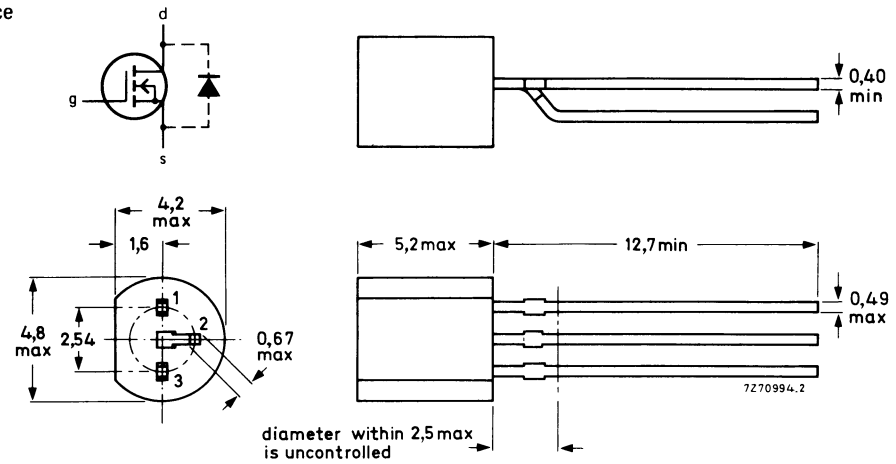
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig. 4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4 ns
		max.	10 ns
	t_{off}	typ.	15 ns
		max.	25 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

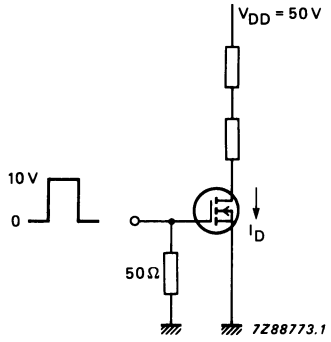


Fig. 2 Switching times test circuit.

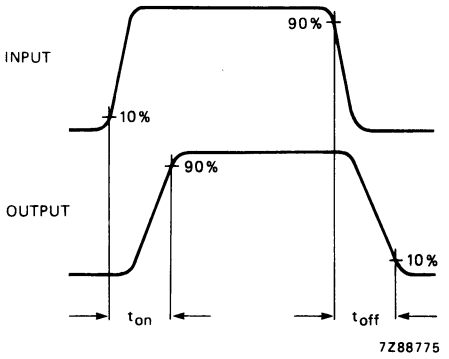


Fig. 3 Input and output waveforms.

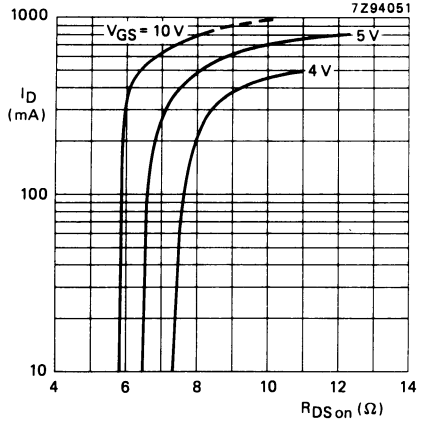


Fig. 4 T_j = 25 °C; typical values.

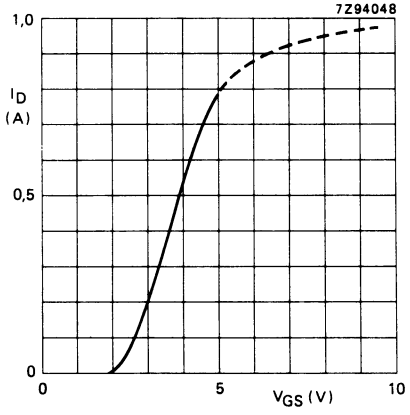


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

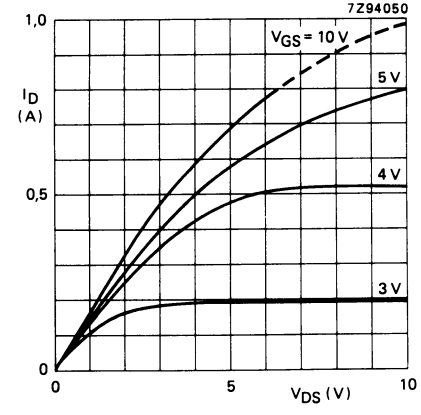


Fig. 6 T_j = 25 °C; typical values.

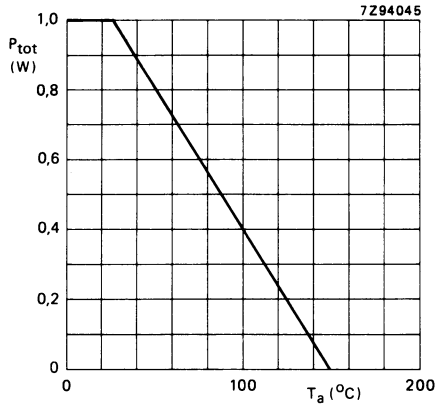


Fig. 7 Power derating curve.

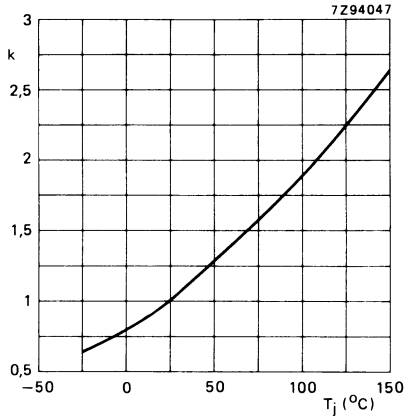


Fig. 8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; at 400 mA/10 V; typical values.

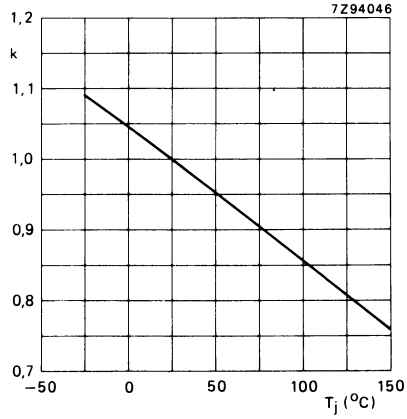


Fig. 9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

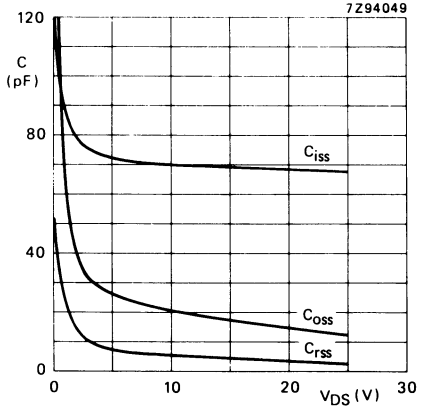


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

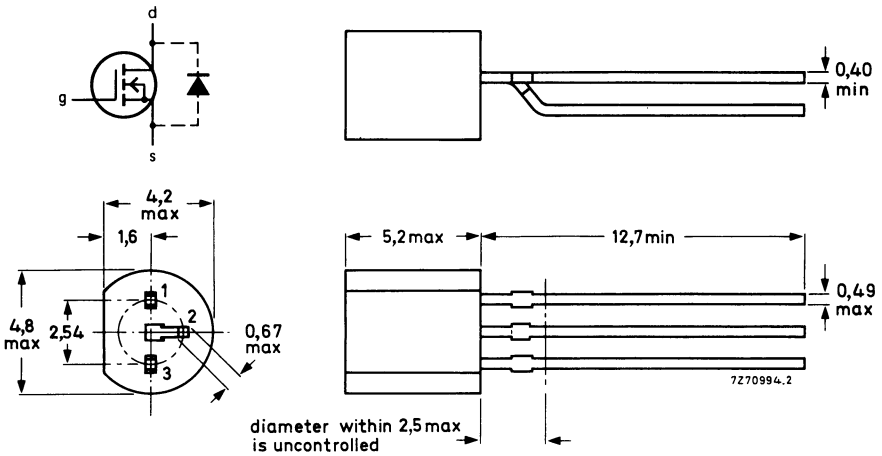
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180 V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 V 2.4 V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	50 pF 65 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	6 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

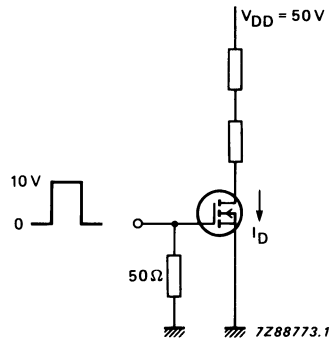


Fig. 2 Switching times test circuit.

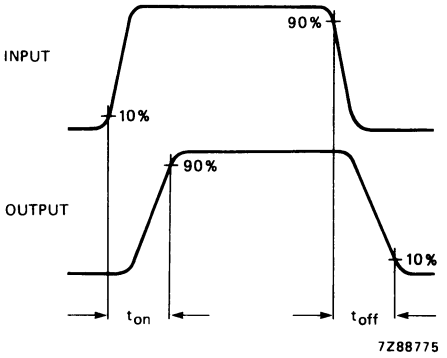


Fig. 3 Input and output waveforms.

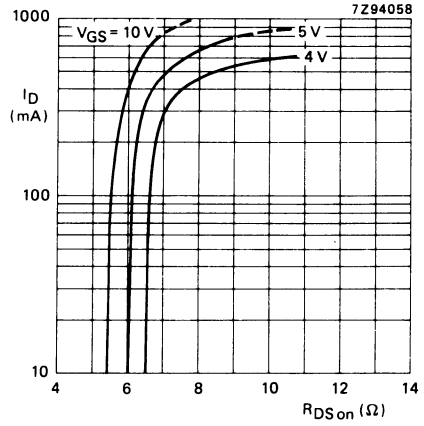


Fig. 4 T_j = 25 °C; typical values.

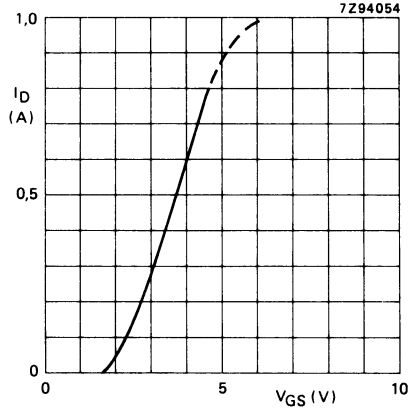


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

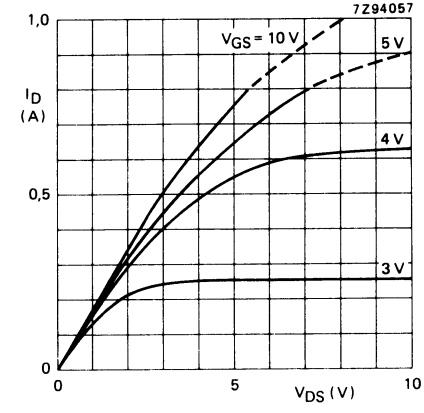


Fig. 6 T_j = 25 °C; typical values.

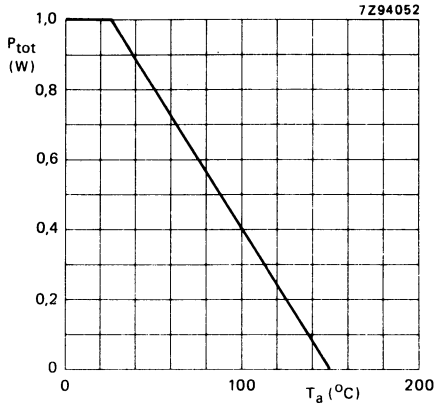


Fig. 7 Power derating curve.

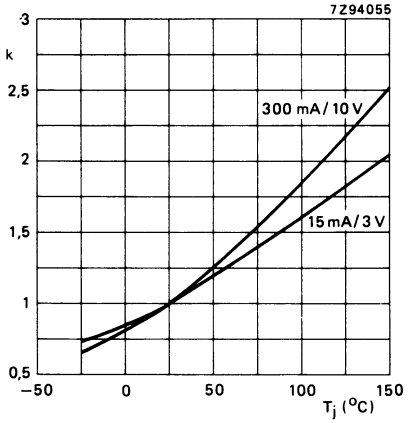


Fig. 8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typical values.

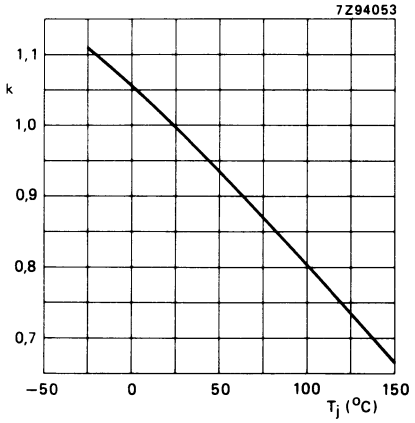


Fig. 9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 0,1 mA; typical values.

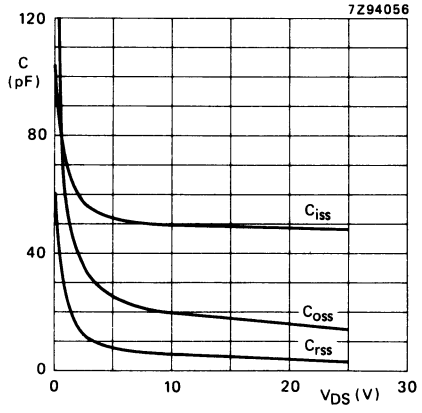


Fig. 10 $T_j = 25\,^{o}C$; $V_{GS} = 0$; f = 1 MHz; typical values.

HIGH-VOLTAGE N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance $I_D = 250$ mA; $V_{DS} = 20$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	400 mS

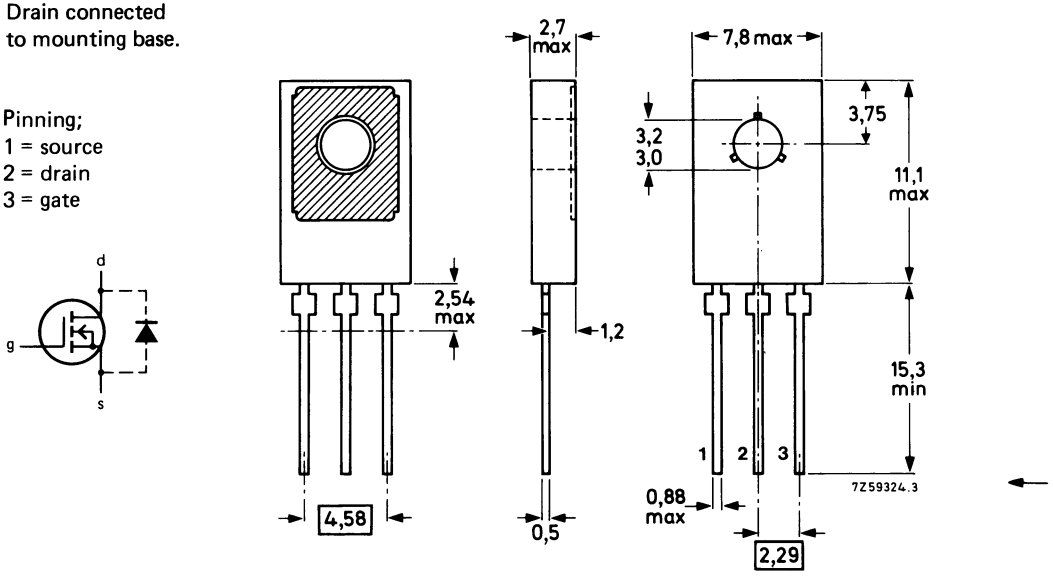
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.

Pinning;
1 = source
2 = drain
3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Drain current (peak)	I_{DM}	max.	1,5 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Storage temperature	T_{stg}	−65 to	+150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$		100 K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$		5 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	450 V
Drain-source leakage current $V_{DS} = 350$ V; $V_{GS} = 0$	I_{DSS}	<	25 μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	>	2,0 V
		<	4,0 V
Drain-source ON-resistance (see Fig. 4) $I_D = 100$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	10 Ω
		<	14 Ω
$I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance at f = 1 kHz $I_D = 250$ mA; $V_{DS} = 20$ V	$\lvert y_{fs} \rvert$	typ.	400 mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ.	75 pF
		<	100 pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ.	25 pF
		<	35 pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	3 pF
		<	5 pF
Switching times (see Figs 2 and 3) $I_D = 100$ mA; $V_{DS} = 200$ V; $V_{GS} = 0$ to 10 V	t_{on}	<	10 ns
	t_{off}	<	100 ns

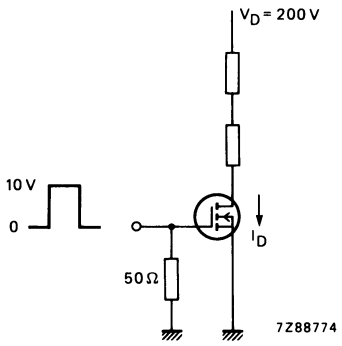


Fig. 2 Switching times test circuit.

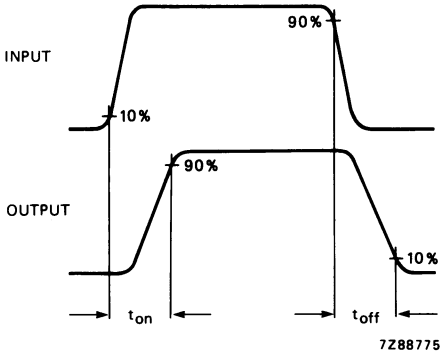


Fig. 3 Input and output waveforms.

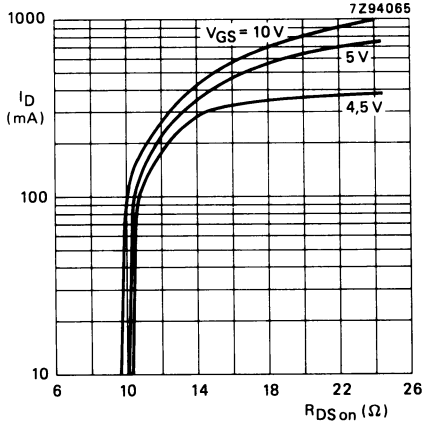


Fig. 4 T_j = 25 °C; typical values.

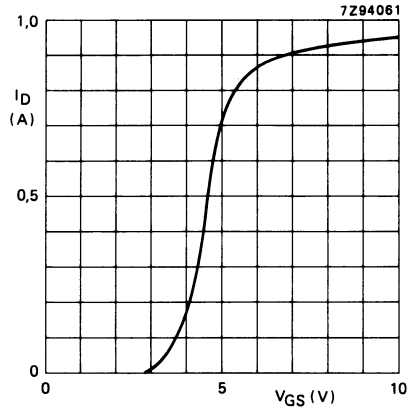


Fig. 5 T_j = 25 °C; V_{DS} = 20 V; typical values.

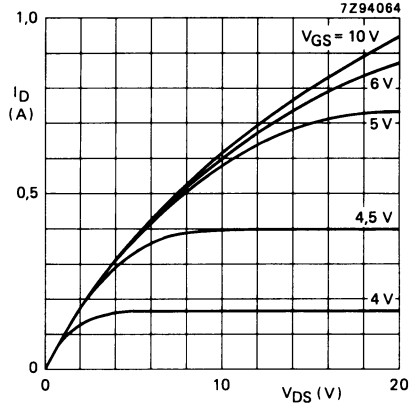


Fig. 6 T_j = 25 °C; typical values.

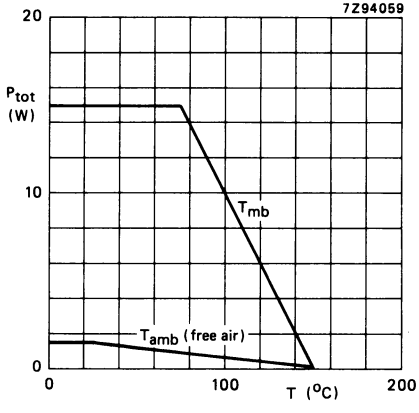


Fig. 7 Power derating curve.

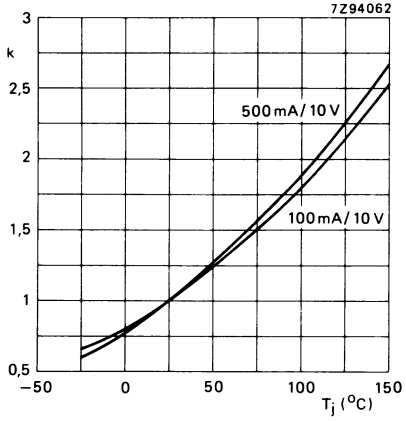


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typical values.

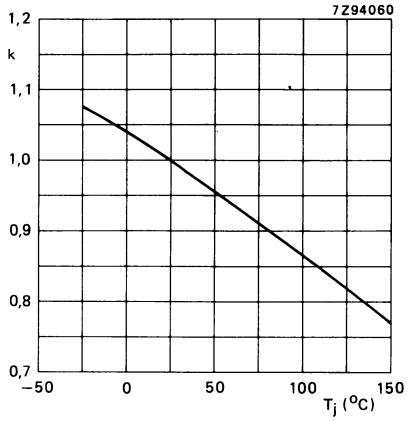


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

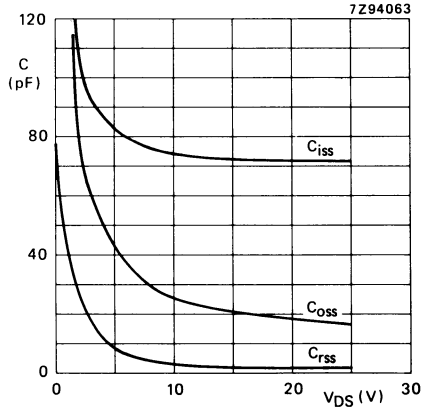


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Low $R_{DS\ on}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS

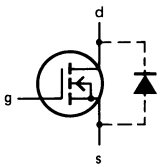
MECHANICAL DATA

Dimensions in mm

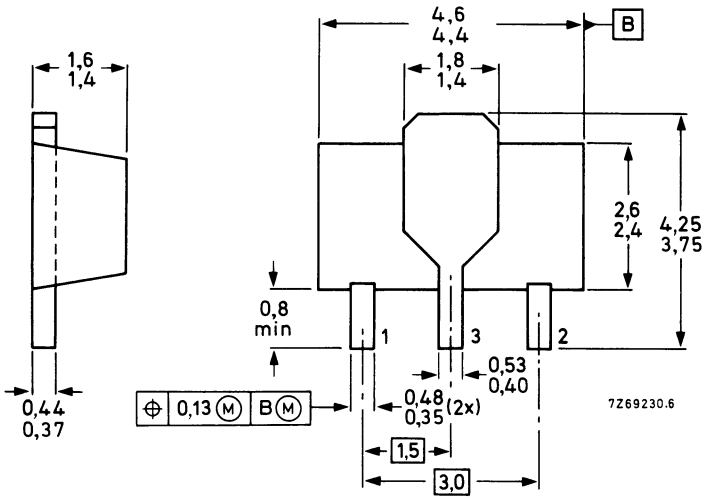
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: KM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistors mounted on a substrate with surface area of 2.5 cm^2 and thickness of 0.7 mm.

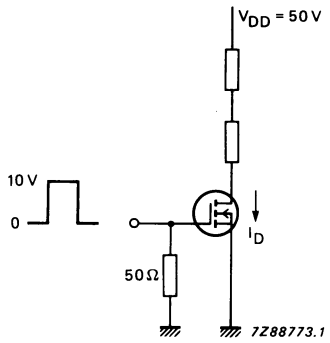


Fig.2 Switching times test circuit.

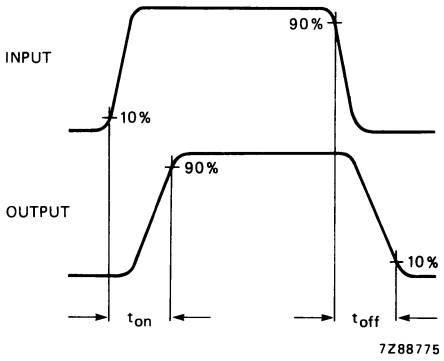


Fig.3 Input and output waveforms.

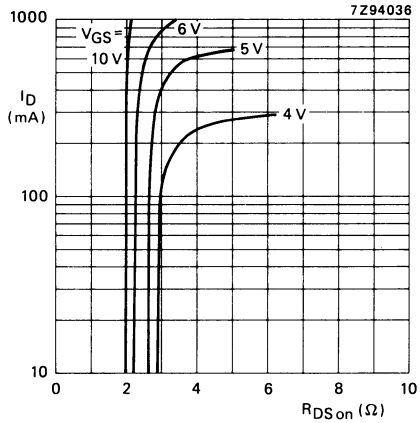


Fig.4 T_j = 25 °C; typical values.

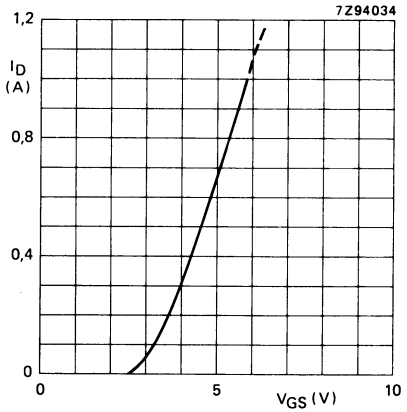


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

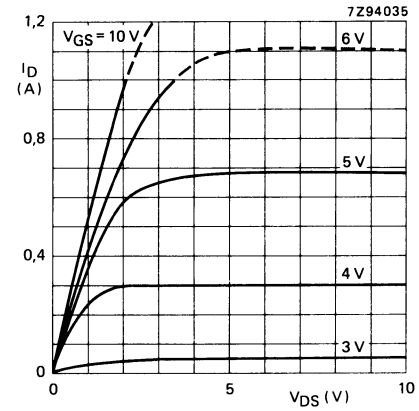


Fig.6 T_j = 25 °C; typical values.

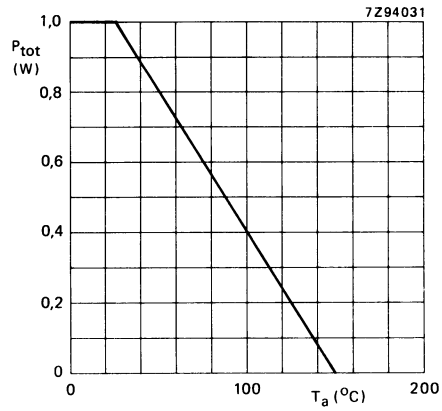


Fig.7 Power derating curve.

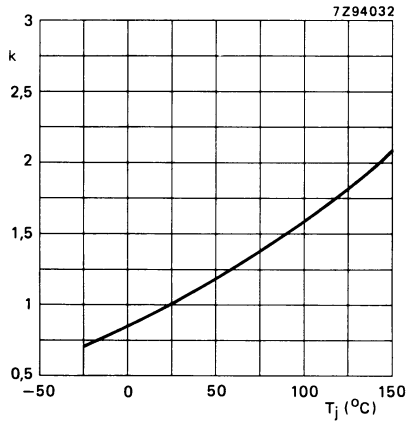


Fig.8 $k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\,^{\circ}C}$; typ. values. at 500 mA/10 V.

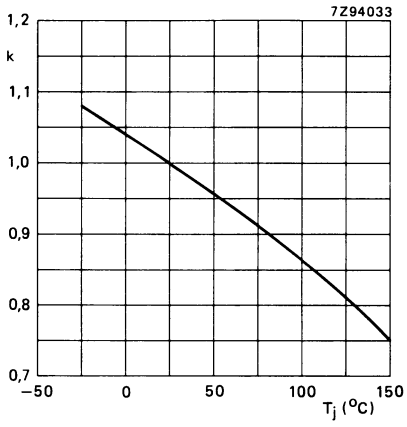


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,^{\circ}C}$; $V_{GS(th)}$ at 1 mA; typical values.

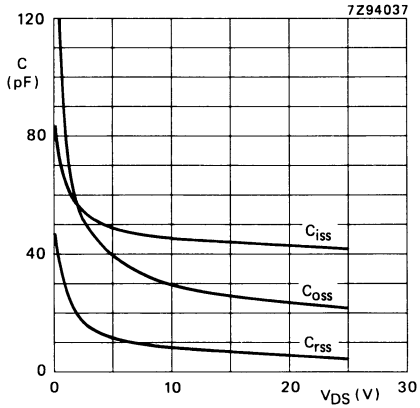


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 Ω 10 Ω	
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V	$\lvert y_{fs} \rvert$	typ.	150	mS

MECHANICAL DATA

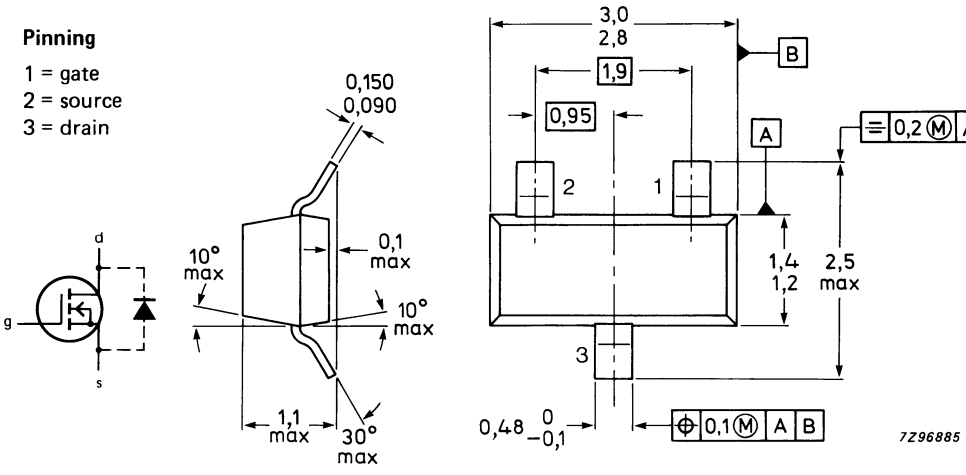
Dimensions in mm

Marking: 02

Fig.1 SOT23.

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}	−65 to	+ 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 pF 6 pF
Switching times (see Figs 2 and 3) I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	4 ns 10 ns

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

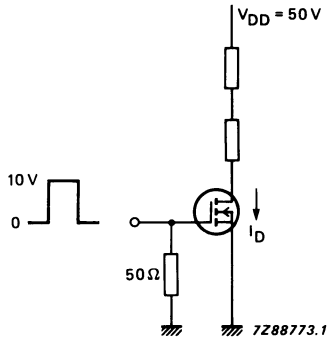


Fig.2 Switching times test circuit.

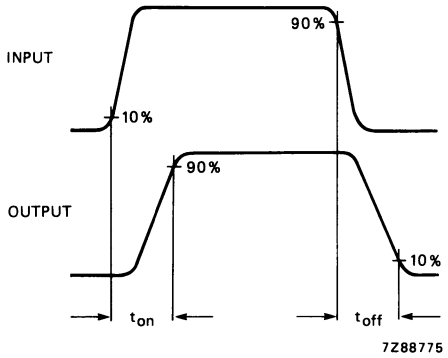


Fig.3 Input and output waveforms.

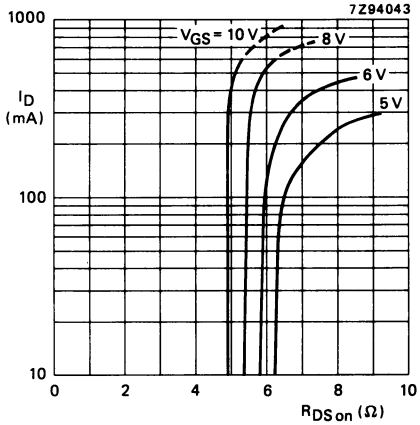


Fig.4 T_j = 25 °C; typical values.

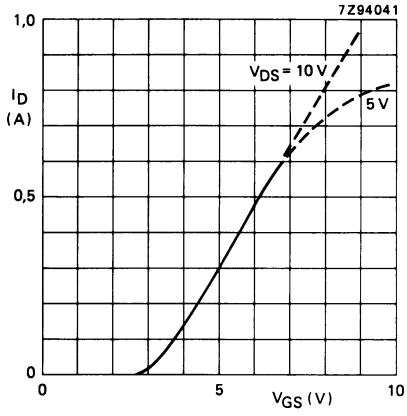


Fig.5 T_j = 25 °C; typical values.

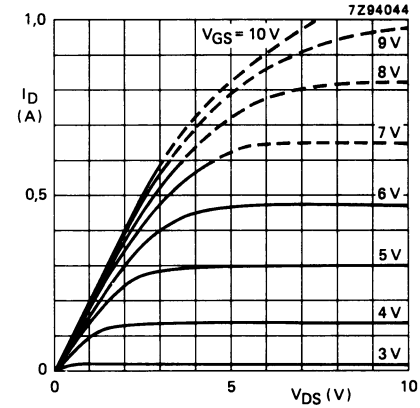


Fig.6 T_j = 25 °C; typical values.

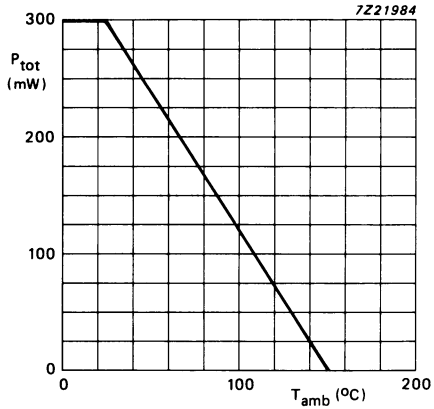


Fig.7 Power derating curve.

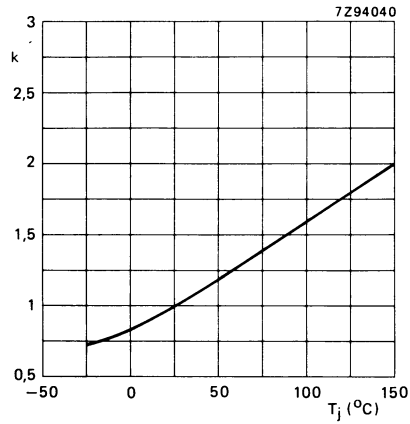


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typ. values at 150 mA/5 V.

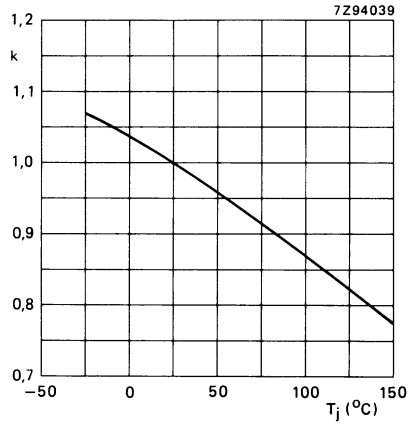


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

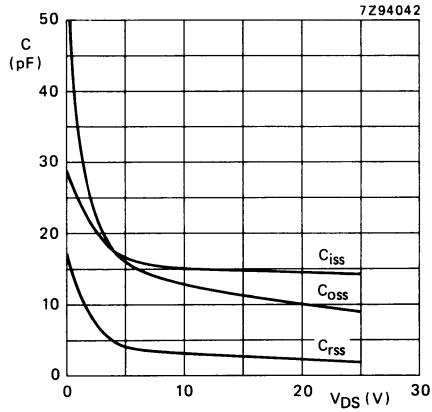


Fig.10 $T_j = 25\,^{o}C$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

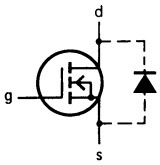
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

MECHANICAL DATA

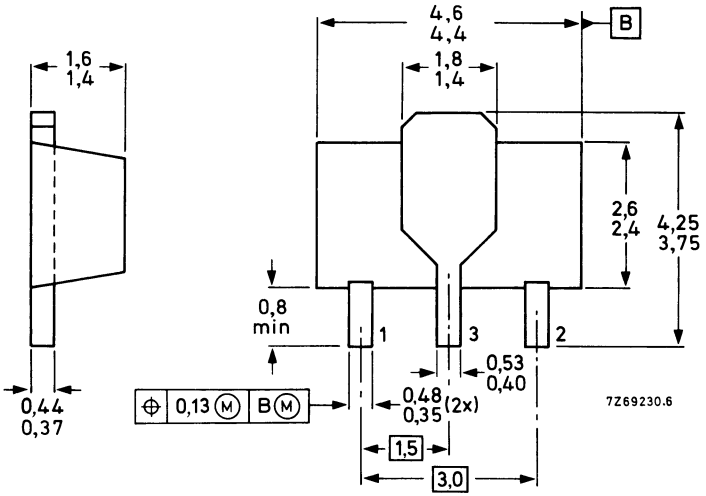
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



Marking: KN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 12	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 90	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	15 25	ns ns

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

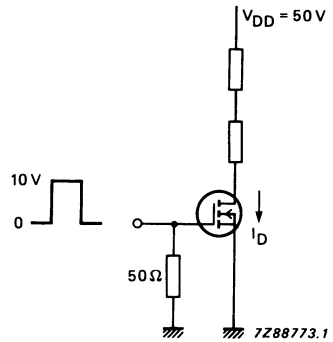


Fig. 2 Switching times test circuit.

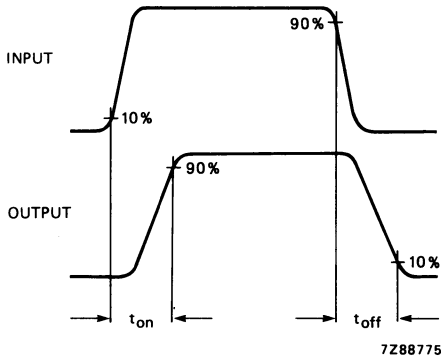


Fig. 3 Input and output waveforms.

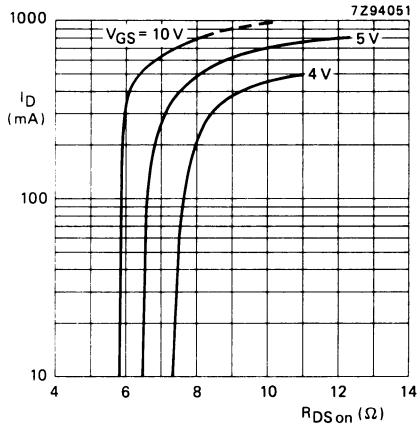


Fig. 4 T_j = 25 °C; typical values.

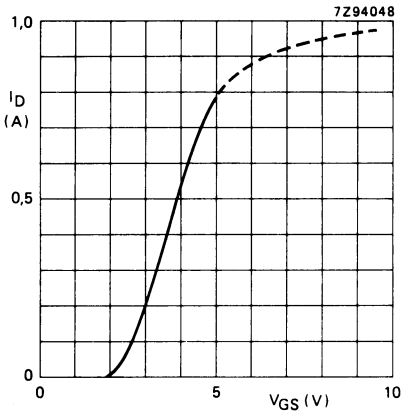


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

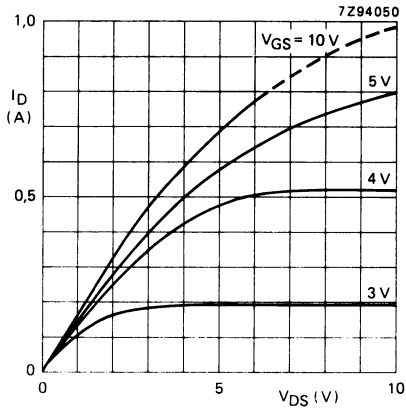


Fig. 6 T_j = 25 °C; typical values.

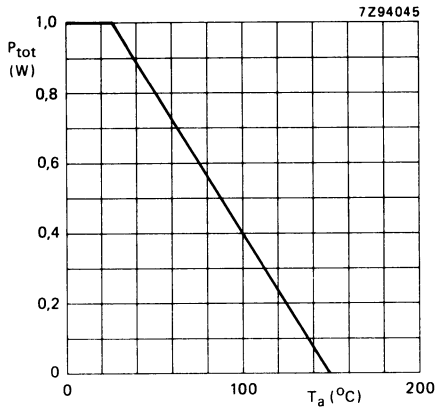


Fig. 7 Power derating curve.

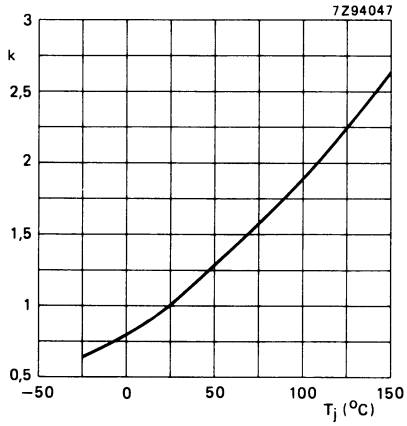


Fig. 8 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; at 400 mA/10 V; typical values.

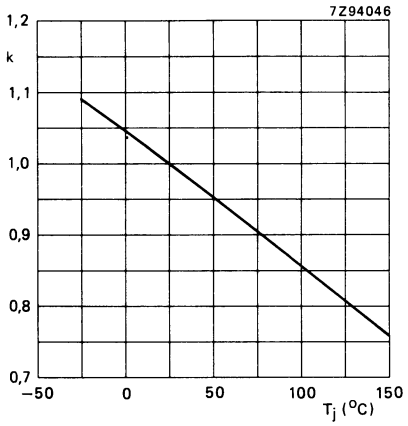


Fig. 9 $k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

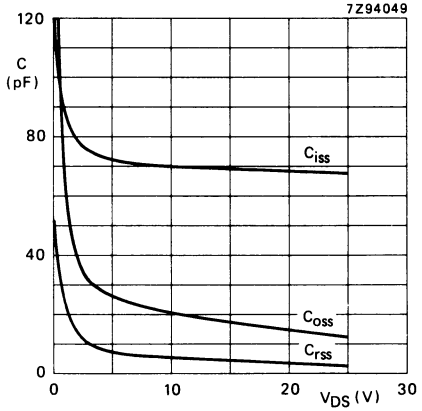


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS

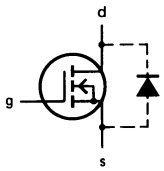
MECHANICAL DATA

Dimensions in mm

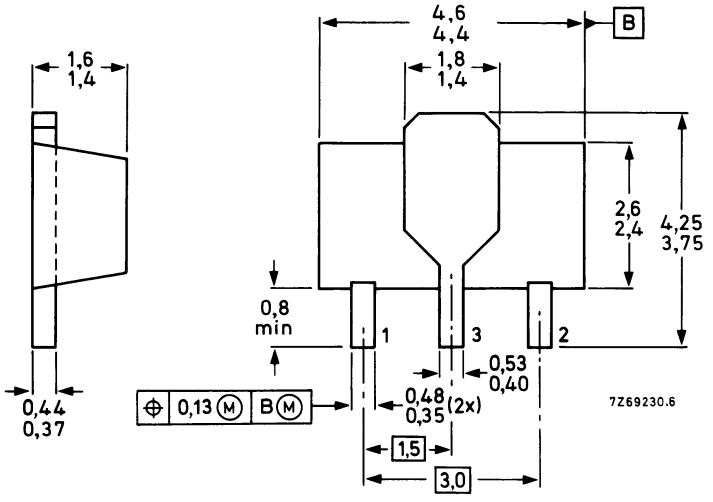
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: K0



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180	V
Drain-source leakage current				
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.7	V
		max.	2.7	V
Drain-source ON-resistance				
I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7	Ω
		max.	10	Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	50	pF
		max.	65	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	6	pF
		max.	10	pF
Switching times (see Figs 2 and 3)				
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	max.	10	ns
	t_{off}	max.	15	ns

1. Transistors mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

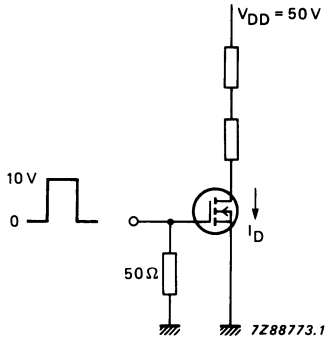


Fig.2 Switching times test circuit.

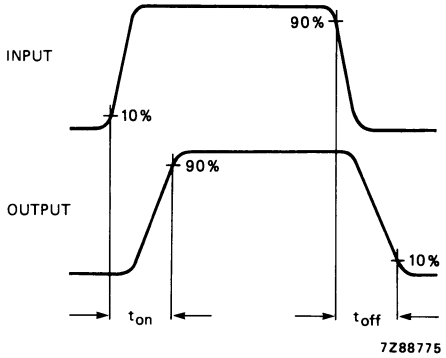


Fig.3 Input and output waveforms.

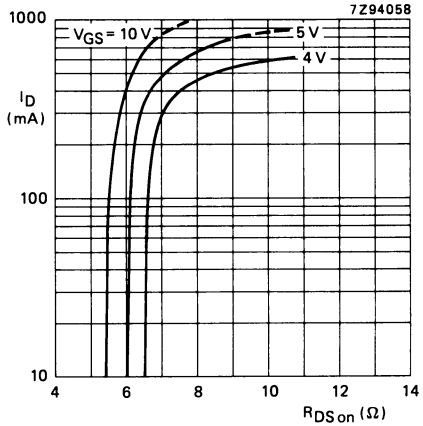


Fig.4 T_j = 25 °C; typical values.

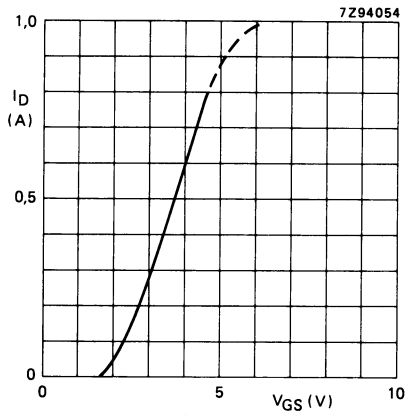


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

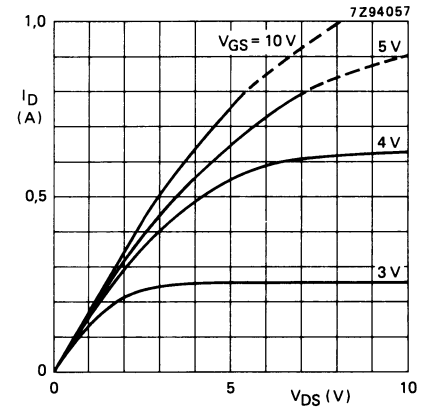


Fig.6 T_j = 25 °C; typical values.

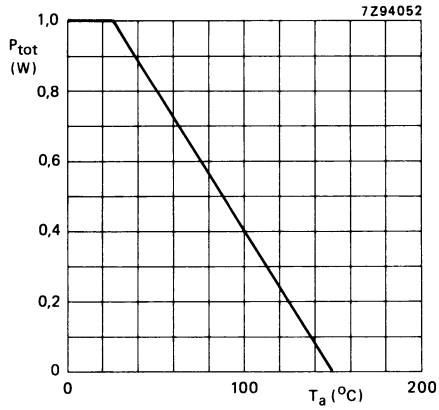


Fig.7 Power derating curve.

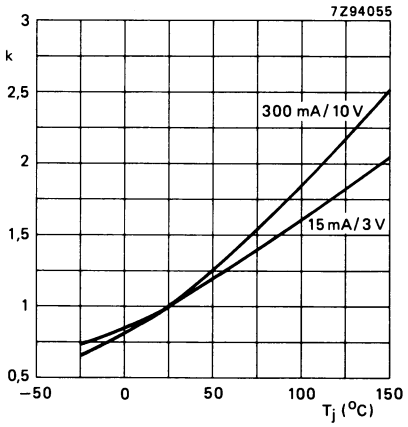


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\ ^oC}$; typical values.

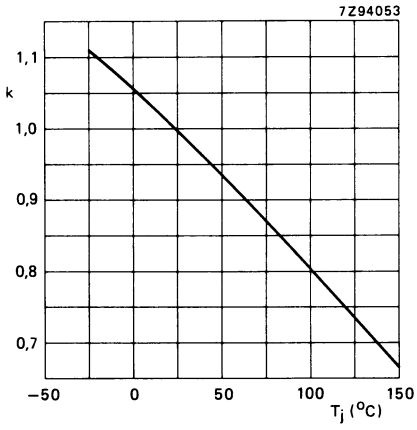


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\ ^oC}$; $V_{GS(th)}$ at 0.1 mA; typical values.

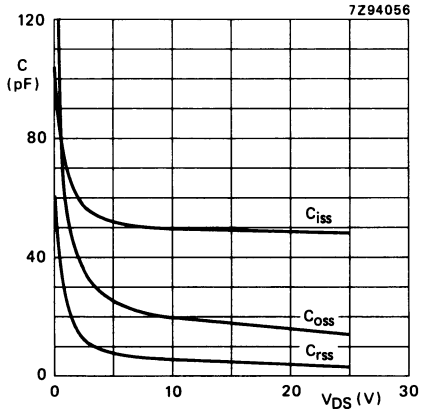


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-39 envelope designed for application in motor controls, power supplies etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	±20 V
Drain current (d.c.)	I_D	max.	2,0 A
Total power dissipation up to T_C = 25 °C	P_{tot}	max.	10 W
Drain-source on-state resistance I_D = 1,5 A; V_{GS} = 10 V	$R_{DS(ON)}$	typ. <	1,8 Ω 2,0 Ω
Transfer admittance I_D = 1,5 A; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ.	0,8 S

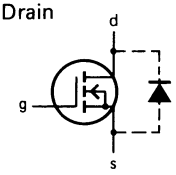
MECHANICAL DATA

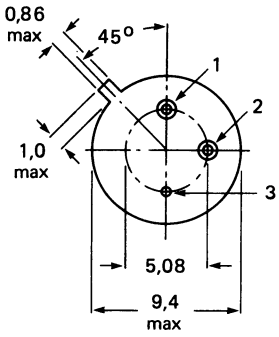
Dimensions in mm

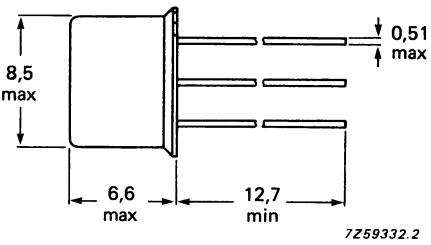
Fig. 1 TO-39.

Pinning:

1 = Source
2 = Gate
3 = Drain







Accessories: 56245 (distance disc)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	±20 V
Drain current (d.c.)	I_D	max.	2,0 A
Drain current (peak)	I_{DM}	max.	5,0 A
Total power dissipation up to T_C = 25 °C	P_{tot}	max.	10 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	12,5 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	<	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100 nA
Gate threshold voltage I_D = 1,0 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	1,0 V 3,0 V
Drain-source on-state resistance I_D = 1,5 A; V_{GS} = 10 V	$R_{DS(ON)}$	typ. <	1,8 Ω 2,0 Ω
Transfer admittance I_D = 1,5 A; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ.	0,8 S
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	120 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	40 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	9 pF
Switching times I_D = 1,5 A; V_{DD} = 75 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	< <	35 ns 50 ns

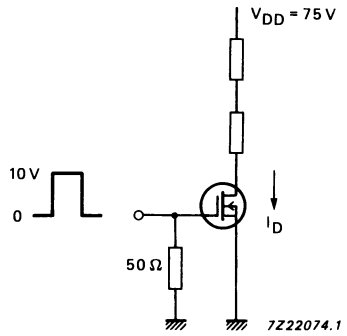


Fig. 2 Switching times test circuit.

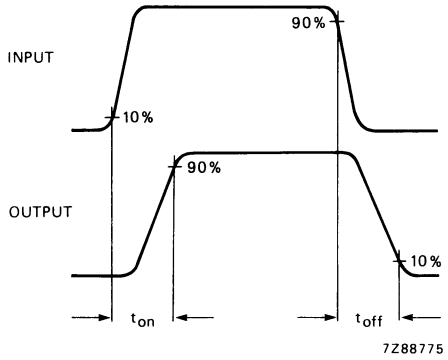


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-18 package and designed for use as line current interrupter in telephone sets and for application in relay, high speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to $T_c = 25$ °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance $I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6 Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250 mS

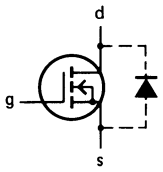
MECHANICAL DATA

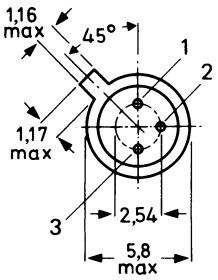
Dimensions in mm

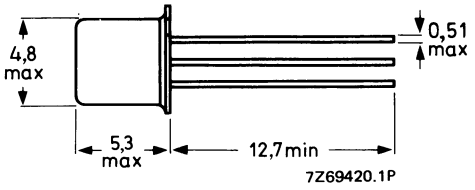
Fig.1 TO-18.

Pinning

1 = Source
2 = Gate
3 = Drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.4 W
Total power dissipation up to T_c = 25 °C	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	310 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180 V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 V 2.7 V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	50 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	6 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

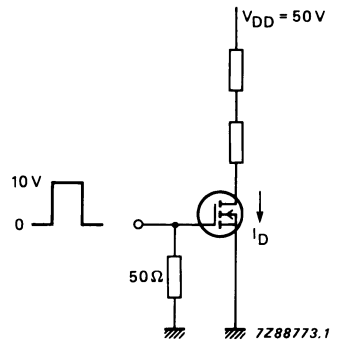


Fig.2 Switching times test circuit.

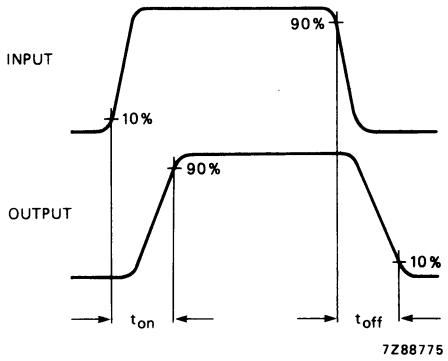


Fig.3 Input and output waveforms.

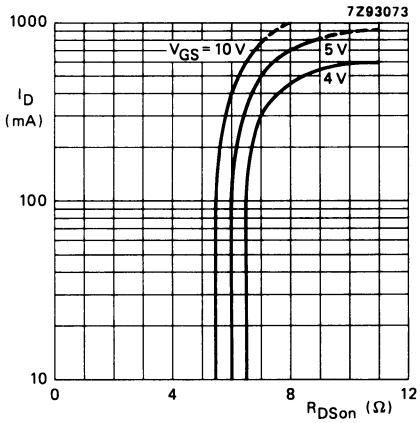


Fig.4 T_j = 25 °C; typical values.

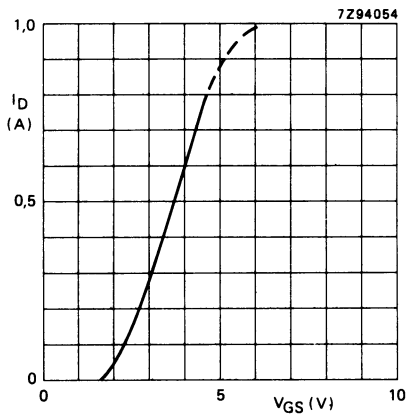


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

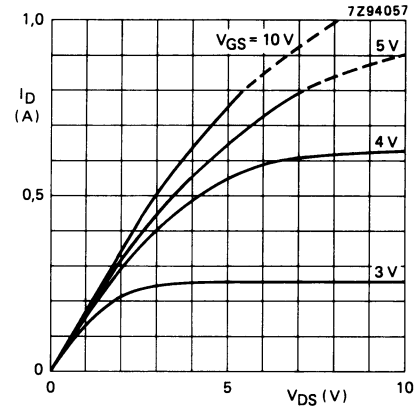


Fig.6 T_j = 25 °C; typical values.

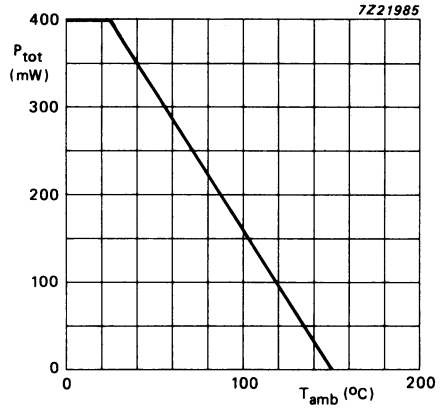


Fig.7 Power derating curve.

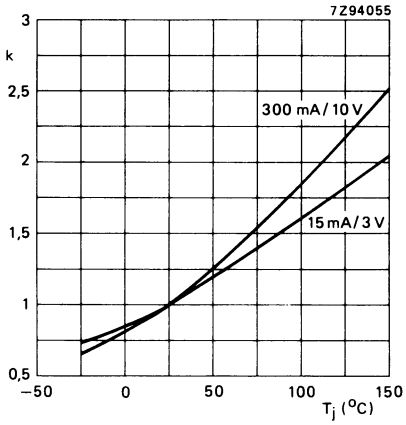


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\ ^oC}$; typical values.

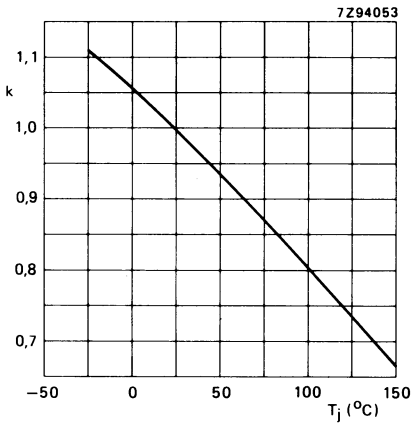


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\ ^oC}$; $V_{GS(th)}$ at 0.1 mA; typical values.

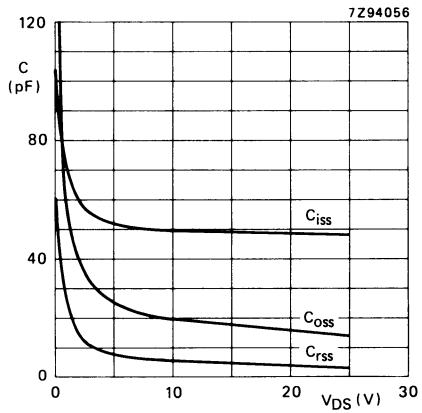


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

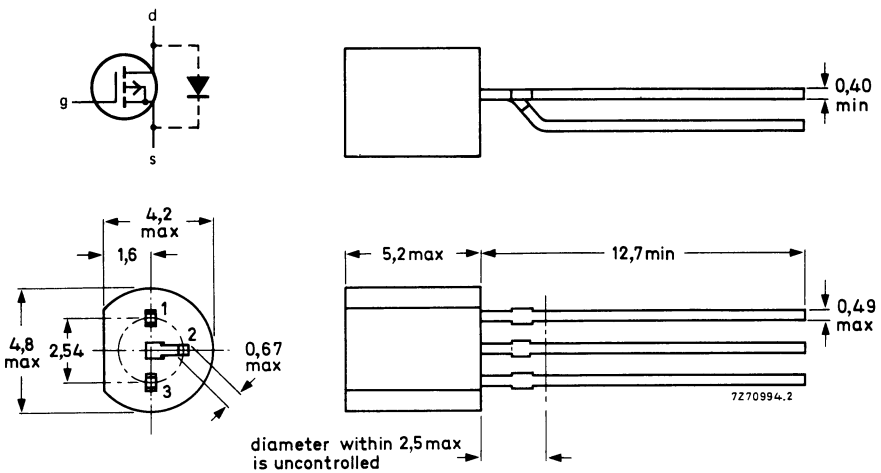
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
→ Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
→ $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current			
$-V_{DS}$ = 45 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage			
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5 V
		max.	3.5 V
Drain-source ON-resistance			
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ.	4.5 Ω
		max.	6 Ω
Transfer admittance			
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz			
→ $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	55 pF
		max.	70 pF
Output capacitance at f = 1 MHz			
→ $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	30 pF
		max.	45 pF
Feedback capacitance at f = 1 MHz			
→ $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	8 pF
		max.	12 pF
Switching times (see Figs 2 and 3)			
→ $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4 ns
	t_{off}	typ.	20 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

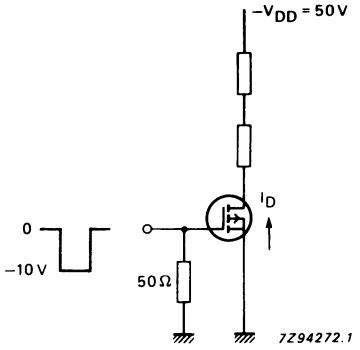


Fig.2 Switching times test circuit.

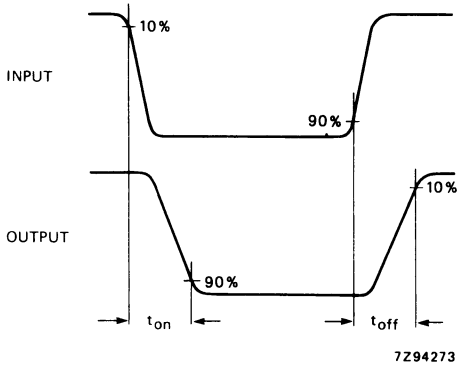


Fig.3 Input and output waveforms.

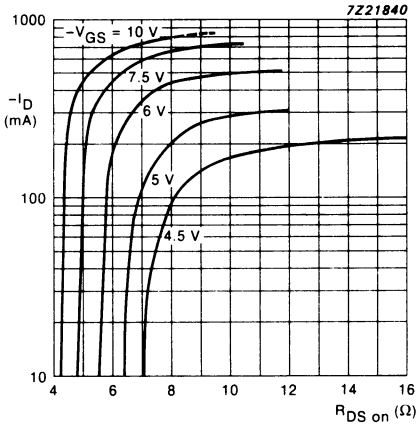


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

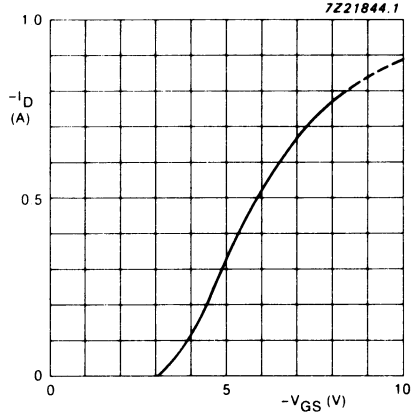


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

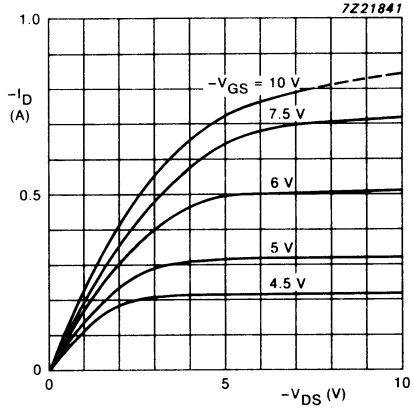


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENCHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125	mS

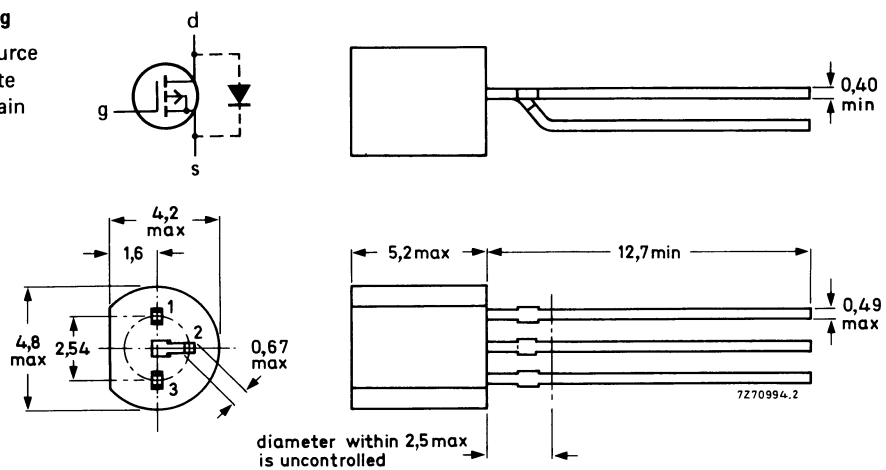
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	50 V
Drain-source leakage current $-V_{DS}$ = 40 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 Ω 10 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

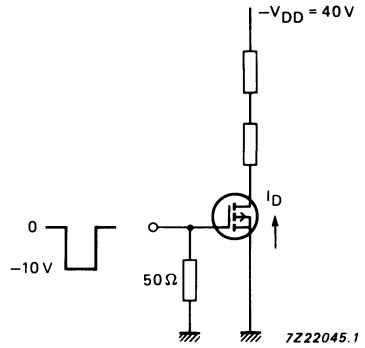


Fig.2 Switching times test circuit.

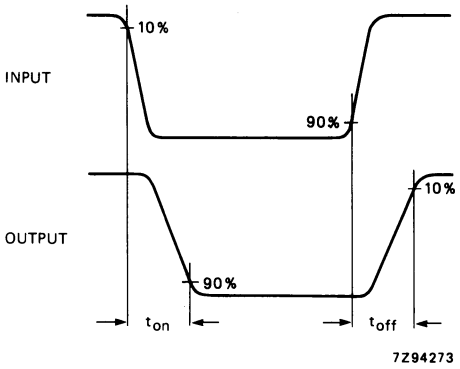


Fig.3 Input and output waveforms.

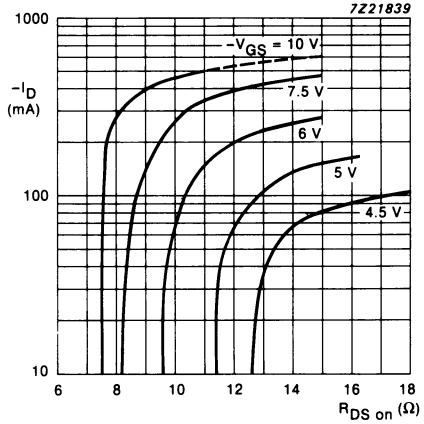


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

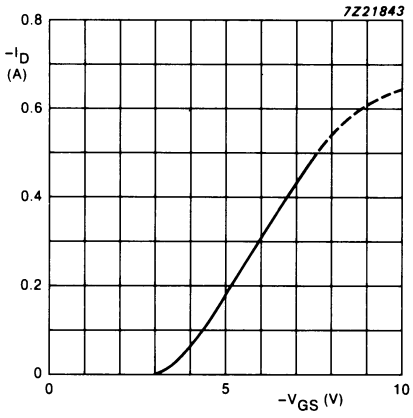


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

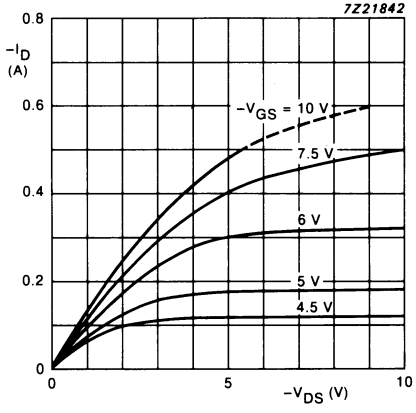


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

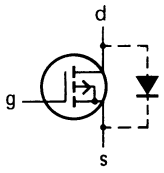
Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 6	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200	mS

MECHANICAL DATA

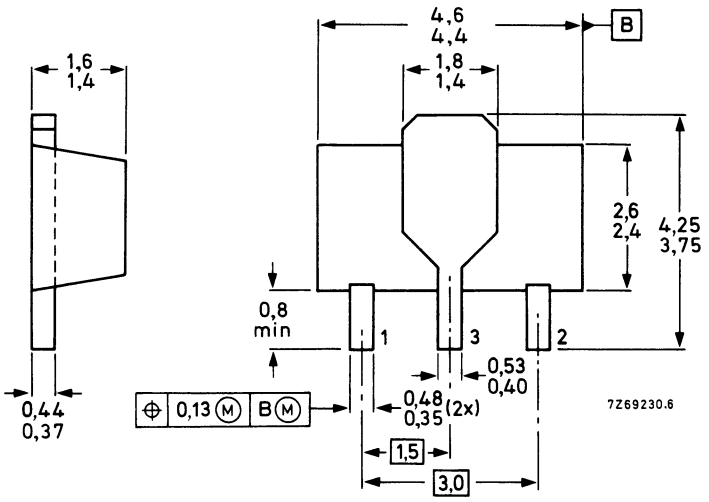
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



marking: LM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 45 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

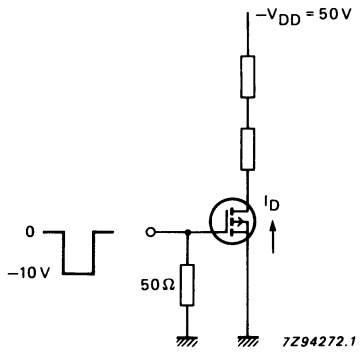


Fig.2 Switching times test circuit.

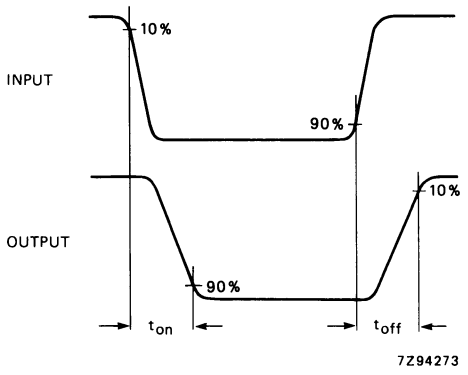


Fig.3 Input and output waveforms.

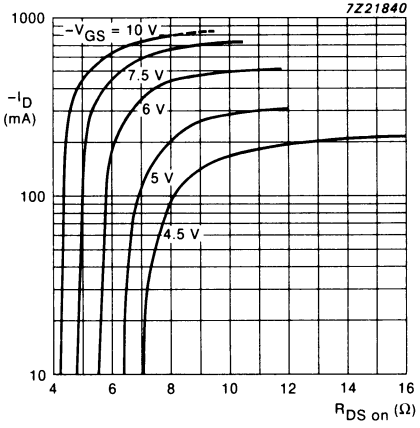


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

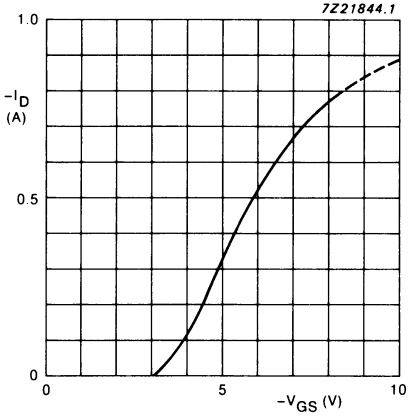


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

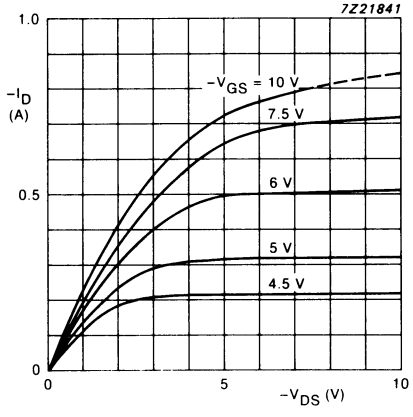


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ.	10 Ω 7.5 Ω	
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125	mS

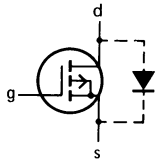
MECHANICAL DATA

Dimensions in mm

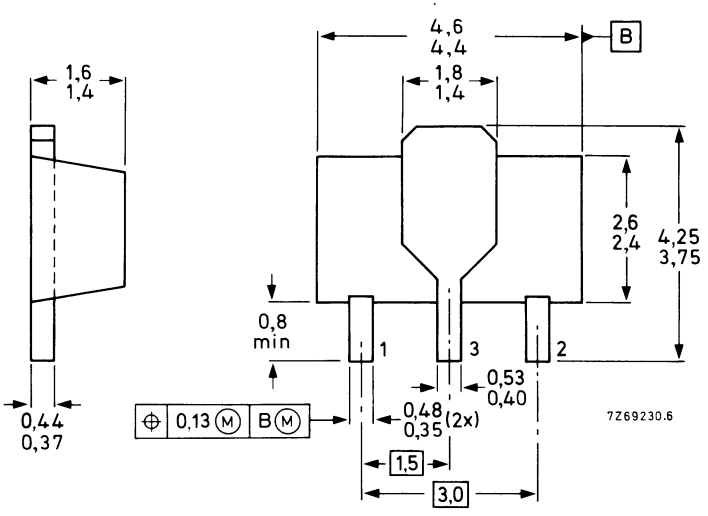
Fig. 1 SOT89.

Pinning:

1 = source
2 = gate
3 = drain



Marking: LN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	50 V
Drain-source leakage current $-V_{DS}$ = 1 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ..	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm²; thickness = 0,7 mm.

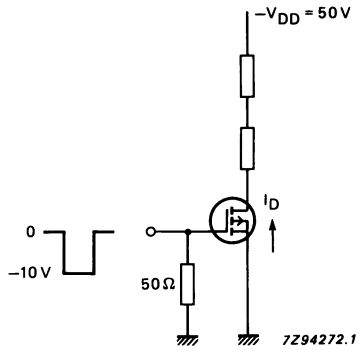


Fig. 2 Switching times test circuit.

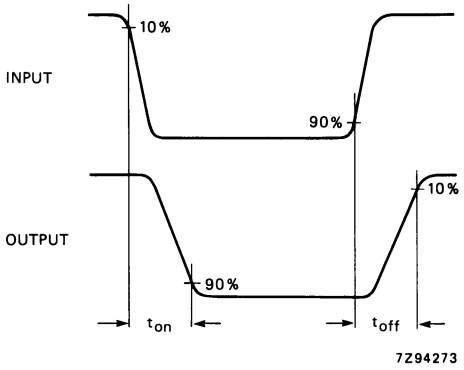


Fig. 3 Input and output waveforms.

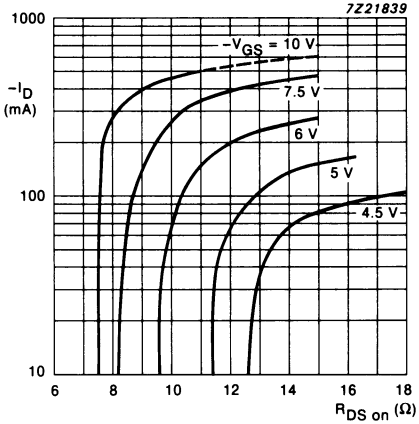


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

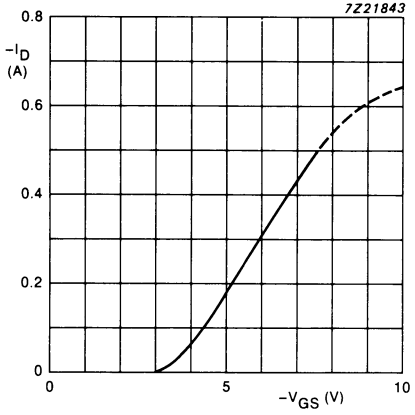


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

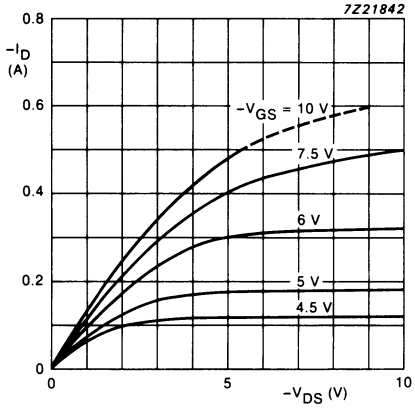


Fig.6 Output characteristics; T_j = 25 °C; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistors, in TO-92 variant envelopes and designed for application as low power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	20	20	V
Drain current (DC)	I_D	max.	0,75	0,5	0,5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	1	1	W
Drain-source on-state resistance I_D = 1.0 A; V_{GS} = 10 V	$R_{DS\,on}$	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance I_D = 0.5 A; V_{DS} = 25 V	$\|y_{fs}\|$	min.	170	170	170	mS

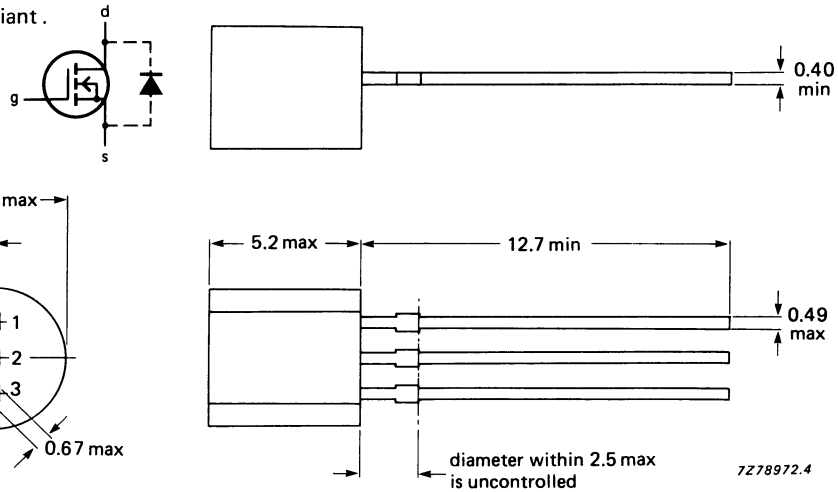
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = Drain
2 = Gate
3 = Source



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
→ Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	20	20	V
Drain current (DC)	I_D	max.	0.75	0.5	0.5	A
Drain current (peak)	I_{DM}	max.		1.0		A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		1		W
Storage temperature range	T_{stg}			−65 to +150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=		125		K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PH6659	PH6660	PH6661	
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	35	60	90	V
Drain-source leakage current at V_{DS} = V_{DS} max; V_{GS} = 0	I_{DSS}	max.	10	10	10	μA
Gate-source leakage current at V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	100	100	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	0.8	0.8	V
		max.	2.0	2.0	2.0	V
On-state drain current V_{DS} = 25 V; V_{GS} = 10 V	$I_{D(ON)}$	min.	1.0	1.0	1.0	A
		typ.	2.0	2.0	2.0	A
Drain-source on-state resistance I_D = 0.3 A; V_{GS} = 5 V	$R_{DS\ on}$	typ.	1.5	1.8	2.4	Ω
		max.	5.0	5.0	5.3	Ω
I_D = 1.0 A; V_{GS} = 10 V	$R_{DS\ on}$	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
→ Transfer admittance I_D = 0.5 A; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	170	170	170	mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	50	50	50	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	50	40	40	pF

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

			PH6659	PH6660	PH6661
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	15	15	15 pF
Switching times I_D = 0,5 A; V_{DD} = 25 V; V_{GS} = 0 to 10 V	t_{on}	max.	10	10	10 ns
	t_{off}	max.	15	15	15 ns

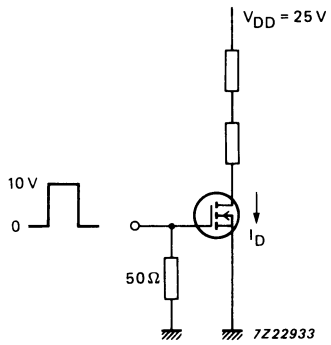


Fig. 2 Switching times test circuit.

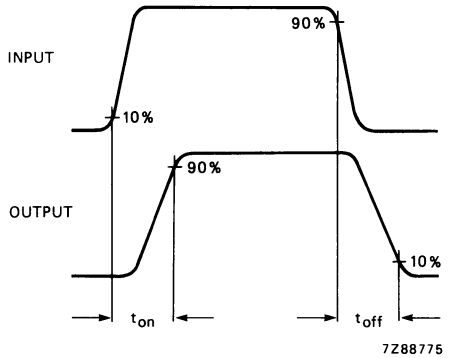


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.5 5.0	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min. typ.	100 200	mS mS

MECHANICAL DATA

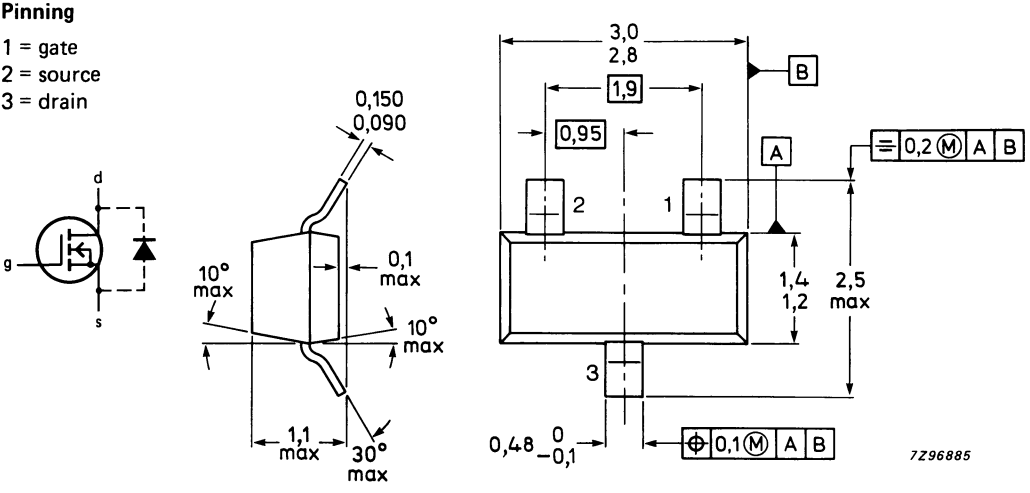
Dimensions in mm

Fig.1 SOT23.

Marking code:
PMBF170 = KX

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300 mW (note 1)
		max.	250 mW (note 2)
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min. typ.	60 V 90 V
Drain-source leakage current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500 nA
V_{DS} = 48V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 3.0 V
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\ on}$	typ. max.	2.5 Ω 5.0 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ. max.	25 pF 40 pF
Output capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ. max.	22 pF 30 pF
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ. max.	6 pF 10 pF

Notes

1. Mounted on ceramic substrate measuring 10 mm x 8 mm x 0.7 mm.
2. Mounted on printed circuit board.

Switching times

V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V

t_{on}	max.	10	ns
t_{off}	max.	15	ns

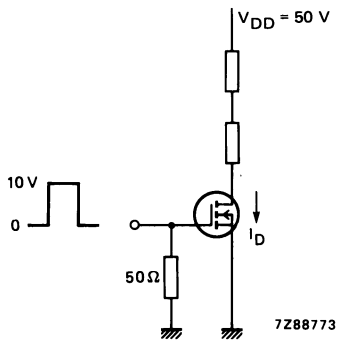


Fig.2 Switching times test circuit.

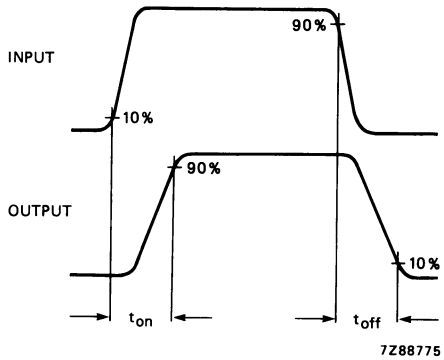


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Total power dissipation up to T_c = 25 °C	P_{tot}	max.	6.25	6.25	6.25	W
Drain-source ON-resistance I_D = 1.0 A; V_{GS} = 10 V	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance I_D = 0.5 A; V_{DS} = 25 V	$\|y_{fs}\|$	max.	170	170	170	mS

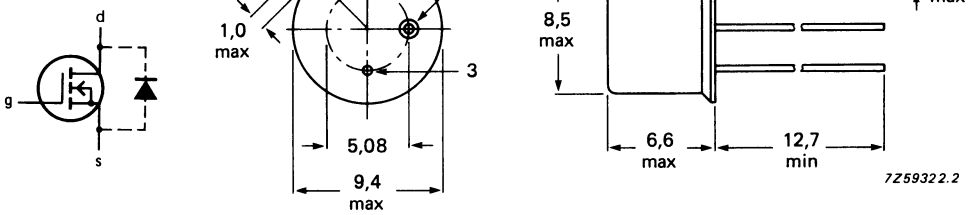
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.

Pinning:

1 = Source
2 = Gate
3 = Drain



Maximum lead diameter is guaranteed only for 12.7 mm

Accessories: 56245 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Drain current (peak) (note 1)	I_{DM}	max.		3,0		A
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.		6.25		W
Storage temperature range	T_{stg}			−65 to + 150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=		20		K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			2N6659	2N6660	2N6661	
Drain-source breakdown voltage $I_D = 10\ \mu A; V_{GS} = 0$	$V_{(BR)DSS}$	min.	35	60	90	V
Drain-source leakage current at $V_{DS} = V_{DSmax}; V_{GS} = 0$	I_{DSS}	max.	10	10	10	μA
Gate-source leakage current at $V_{GS} = 15\ V; V_{DS} = 0$	I_{GSS}	max.	100	100	100	nA
Gate threshold voltage $I_D = 1\ mA; V_{DS} = V_{GS}$	$V_{GS(th)}$	min.	0.8	0.8	0.8	V
		max.	2.0	2.0	2.0	V
ON-state drain current $V_{DS} = 25\ V; V_{GS} = 10\ V$	$I_{D(on)}$	min.	1.0	1.0	1.0	A
		typ.	2.0	2.0	2.0	A
Drain-source ON-resistance $I_D = 0.3\ A; V_{GS} = 5\ V$	R_{DSon}	typ.	1.5	1.8	2.4	Ω
		max.	5.0	5.0	5.3	Ω
$I_D = 1.0\ A; V_{GS} = 10\ V$	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance $I_D = 0.5\ A; V_{DS} = 25\ V$	$\lvert y_{fs} \rvert$	min.	170	170	170	mS
Input capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{iss}	max.	50	50	50	pF
Output capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{oss}	max.	50	40	40	pF

Note

1. Pulse conditions: $t_p \leqslant 300\ \mu s; \delta = 0.01$.

		2N6659	2N6660	2N6661	
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss} max.	15	15	15	pF
Switching times I_D = 1.0 A; V_{DD} = 25 V; V_{GS} = 0 to 10 V	t_{on} typ.	5	5	5	ns
	t_{on} max.	10	10	10	ns
	t_{off} typ.	5	5	5	ns
	t_{off} max.	10	10	10	ns

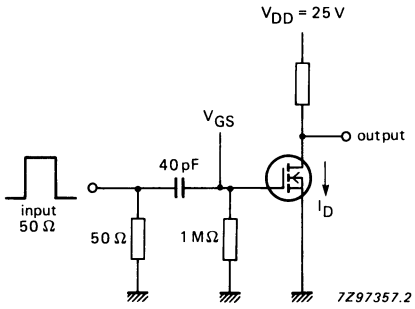


Fig. 2 Switching times test circuit.

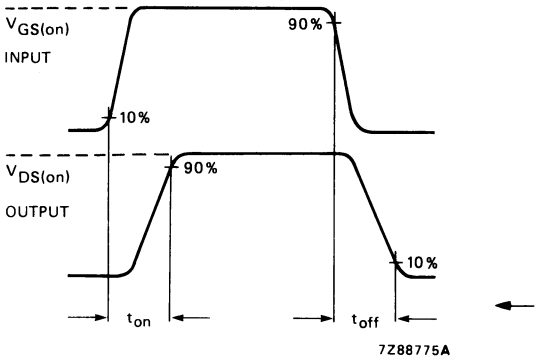
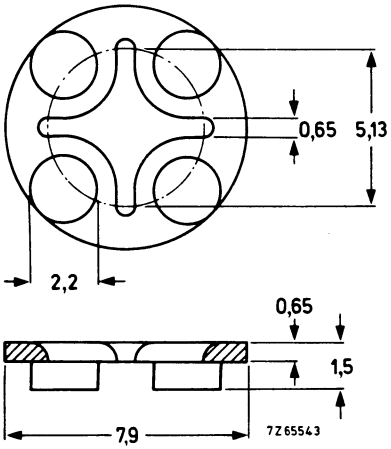


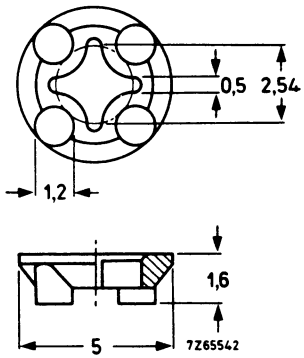
Fig. 3 Input and output waveforms.

MECHANICAL DATA

Dimensions in mm



Distance disc 56245 for TO-5 or TO-39; insulating material.

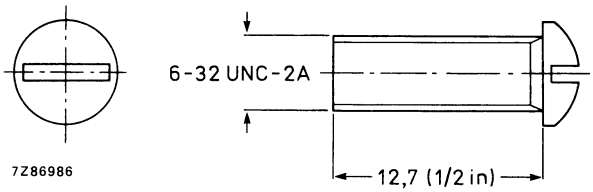


Distance disc 56246 for TO-18 or TO-72; insulating material.

Maximum permissible temperature: 100 °C.

ROUND HEAD SCREW 6-32 UNC-2A

Available, upon request, under type number 56396 or 12 NC code number 9390 298 10xx0.



INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	book	section
BA220	SC01	SD
BA221	SC01	SD
BA223	SC01	T
BA281	SC01	SD
BA314	SC01	Vrg
BA315	SC01	Vrg
BA316	SC01	SD
BA317	SC01	SD
BA318	SC01	SD
BA423	SC01	T
BA423L	SC01	T
BA480	SC01	T
BA481	SC01	T
BA482	SC01	T
BA483	SC01	T
BA484	SC01	T
BA682	SC01/10	T/Mm
BA683	SC01/10	T/Mm
BAS11	SC01	SD
BAS15	SC01	SD
BAS16	SC01/10	SD/Mm
BAS17	SC01/10	Vrg/Mm
BAS19	SC01/10	SD/Mm
BAS20	SC01/10	SD/Mm
BAS21	SC01/10	SD/Mm
BAS28	SC01/10	SD/Mm
BAS29	SC01/10	SD/Mm
BAS31	SC01/10	SD/Mm
BAS32	SC01/10	SD/Mm
BAS32L	SC01/10	SD/Mm
BAS35	SC01/10	SD/Mm
BAS45	SC01	SD
BAS45L	SC01/10	SD/Mm
BAS56	SC01/10	SD/Mm
BAS85	SC01	SD
BAT17	SC01/10	T/Mm
BAT18	SC01/10	T/Mm
BAT54	SC01/10	SD/Mm
BAT74	SC01/10	SD/Mm
BAT81	SC01	T
BAT82	SC01	T
BAT83	SC01	T
BAT85	SC01	T
BAT86	SC01	T
BAV10	SC01	SD
BAV18	SC01	SD
BAV19	SC01	SD
BAV20	SC01	SD
BAV21	SC01	SD
BAV23	SC01/10	SD/Mm
BAV45	SC01	Sp
BAV70	SC01/10	SD/Mm
BAV74	SC01	SD
BAV99	SC01/10	SD/Mm
BAV100	SC01/10	SD/Mm
BAV101	SC01/10	SD/Mm
BAV102	SC01/10	SD/Mm
BAV103	SC01/10	SD/Mm
BAV105	SC01/10	SD/Mm
BAW56	SC01/10	SD/Mm
BAW62	SC01	SD
BAX12	SC01	SD
BAX14	SC01	SD
BAX18	SC01	SD
BAY80	SC01	SD
BB112	SC01	T
BB119	SC01	T
BB130	SC01	T
BB204B	SC01	T
BB204G	SC01	T
BB212	SC01	T
BB215	SC01/10	SD/Mm
BB219	SC01/10	SD/Mm
BB240	SC01/10	T/Mm
BB241	SC01/10	T/Mm

Key to handbook sections

A = Accessories
FET = Field-effect transistors
I = Infrared devices
LED = Light-emitting diodes
LCD = Liquid crystal displays
Mm = Surface-mounted devices
M = Microwave transistors
P = Low-frequency power transistors and modules
PDT = Photodiodes or transistors
Ph = Photoconductive devices
PhC = Photocouplers
PM = PowerMOS transistors
R = Rectifier diodes
RFP = RF power transistors and modules
RT = Triplers
SEN = Semiconductor sensors
SD = Small-signal diodes
Sm = Small-signal transistors
Sp = Special diodes
SP = Low-frequency switching power diodes
St = Rectifier stacks
T = Tuner diodes
Th = Thyristors
Tri = Triacs
TS = Transient suppressor diodes
Vrf = Voltage reference diodes
Vrg = Voltage regulator diodes
WBT = Wideband hybrid IC transistors
WBM = Wideband hybrid IC modules

* series.

type no.	book	section
BB405B	SC01	T
BB417	SC01	T
BB804	SC01/10	T/Mm
BB809	SC01	T
BB909A	SC01	T
BB909B	SC01	T
BB910	SC01	T
BB911	SC01	T
BBY31	SC01/10	T/Mm
BBY39	SC01	T
BBY40	SC01/10	T/Mm
BBY42	SC01	T
BBY62	SC01	T
BC107	SC04	Sm
BC108	SC04	Sm
BC109	SC04	Sm
BC140	SC04	Sm
BC141	SC04	Sm
BC160	SC04	Sm
BC161	SC04	Sm
BC177	SC04	Sm
BC178	SC04	Sm
BC179	SC04	Sm
BC264A	SC07	FET
BC264B	SC07	FET
BC246C	SC07	FET
BC264D	SC07	FET
BC327	SC04	Sm
BC327A	SC04	Sm
BC328	SC04	Sm
BC337	SC04	Sm
BC337A	SC04	Sm
BC338	SC04	Sm
BC368	SC04	Sm
BC369	SC04	Sm
BC375	SC04	Sm
BC376	SC04	Sm
BC516	SC04	Sm
BC517	SC04	Sm
BC546	SC04	Sm
BC547	SC04	Sm
BC548	SC04	Sm
BC549	SC04	Sm
BC550	SC04	Sm
BC556	SC04	Sm
BC557	SC04	Sm
BC558	SC04	Sm
BC559	SC04	Sm
BC560	SC04	Sm
BC617	SC04	Sm
BC618	SC04	Sm
BC635	SC04	Sm
BC636	SC04	Sm
BC637	SC04	Sm
BC638	SC04	Sm
BC639	SC04	Sm
BC640	SC04	Sm
BC807	SC10	Mm
BC808	SC10	Mm
BC817	SC10	Mm
BC818	SC10	Mm
BC846	SC10	Mm
BC847	SC10	Mm
BC848	SC10	Mm
BC849	SC10	Mm
BC850	SC10	Mm
BC856	SC10	Mm
BC857	SC10	Mm
BC858	SC10	Mm
BC859	SC10	Mm
BC860	SC10	Mm
BC868	SC10	Mm
BC869	SC10	Mm
BC875	SC04	Sm
BC876	SC04	Sm
BC877	SC04	Sm
BC878	SC04	Sm
BC879	SC04	Sm
BC880	SC04	Sm
BCF29	SC10	Mm
BCF29R	SC10	Mm
BCF30	SC10	Mm
BCF30R	SC10	Mm
BCF32	SC10	Mm
BCF32R	SC10	Mm
BCF33	SC10	Mm
BCF33R	SC10	Mm
BCF70	SC10	Mm
BCF70R	SC10	Mm
BCF81	SC10	Mm
BCF81R	SC10	Mm
BCP51	SC10	Mm
BCP52	SC10	Mm
BCP53	SC10	Mm
BCP54	SC10	Mm
BCP55	SC10	Mm
BCP56	SC10	Mm
BCP68	SC10	Mm
BCP69	SC10	Mm
BCV26	SC10	Mm
BCV27	SC10	Mm
BCV28	SC10	Mm
BCV29	SC10	Mm
BCV46	SC10	Mm
BCV47	SC10	Mm
BCV48	SC10	Mm
BCV49	SC10	Mm
BCV61	SC10	Mm
BCV62	SC10	Mm
BCV63	SC10	Mm
BCV64	SC10	Mm
BCV65	SC10	Mm
BCV71	SC10	Mm
BCV71R	SC10	Mm
BCV72	SC10	Mm
BCV72R	SC10	Mm
BCW29	SC10	Mm
BCW29R	SC10	Mm
BCW30	SC10	Mm
BCW30R	SC10	Mm
BCW31	SC10	Mm
BCW31R	SC10	Mm
BCW32	SC10	Mm
BCW32R	SC10	Mm
BCW33	SC10	Mm
BCW33R	SC10	Mm
BCW60*	SC10	Mm
BCW61*	SC10	Mm
BCW69	SC10	Mm
BCW69R	SC10	Mm
BCW70	SC10	Mm
BCW70R	SC10	Mm
BCW71	SC10	Mm
BCW71R	SC10	Mm
BCW72	SC10	Mm

type no.	book	section
BCW72R	SC10	Mm
BCW81	SC10	Mm
BCW81R	SC10	Mm
BCW89	SC10	Mm
BCW89R	SC10	Mm
BCX17	SC10	Mm
BCX17R	SC10	Mm
BCX18	SC10	Mm
BCX18R	SC10	Mm
BCX19	SC10	Mm
BCX19R	SC10	Mm
BCX20	SC10	Mm
BCX20R	SC10	Mm
BCX51	SC10	Mm
BCX52	SC10	Mm
BCX53	SC10	Mm
BCX54	SC10	Mm
BCX55	SC10	Mm
BCX56	SC10	Mm
BCX58	SC04	Sm
BCX59	SC04	Sm
BCX70*	SC10	Mm
BCX71*	SC10	Mm
BCX78	SC04	Sm
BCX79	SC04	Sm
BCY56	SC04	Sm
BCY57	SC04	Sm
BCY58	SC04	Sm
BCY59	SC04	Sm
BCY65	SC04	Sm
BCY70	SC04	Sm
BCY71	SC04	Sm
BCY72	SC04	Sm
BCY78	SC04	Sm
BCY79	SC04	Sm
BCY87	SC04	Sm
BCY88	SC04	Sm
BCY89	SC04	Sm
BD131	SC05	P
BD132	SC05	P
BD135	SC05	P
BD136	SC05	P
BD137	SC05	P
BD138	SC05	P
BD139	SC05	P
BD140	SC05	P
BD201	SC05	P
BD201F	SC05	P
BD202	SC05	P
BD202F	SC05	P
BD203	SC05	P
BD203F	SC05	P
BD204	SC05	P
BD204F	SC05	P
BD226	SC05	P
BD227	SC05	P
BD228	SC05	P
BD229	SC05	P
BD230	SC05	P
BD231	SC05	P
BD233	SC05	P
BD234	SC05	P
BD235	SC05	P
BD236	SC05	P
BD237	SC05	P
BD238	SC05	P
BD239	SC05	P
BD239A	SC05	P
BD239B	SC05	P
BD239C	SC05	P
BD240	SC05	P
BD240A	SC05	P
BD240B	SC05	P
BD240C	SC05	P
BD241	SC05	P
BD241A	SC05	P
BD241B	SC05	P
BD241C	SC05	P
BD242	SC05	P
BD242A	SC05	P
BD242B	SC05	P
BD242C	SC05	P
BD243	SC05	P
BD243A	SC05	P
BD243B	SC05	P
BD243C	SC05	P
BD244	SC05	P
BD244A	SC05	P
BD244B	SC05	P
BD244C	SC05	P
BD329	SC05	P
BD330	SC05	P
BD331	SC05	P
BD332	SC05	P
BD333	SC05	P
BD334	SC05	P
BD335	SC05	P
BD336	SC05	P
BD337	SC05	P
BD338	SC05	P
BD433	SC05	P
BD434	SC05	P
BD435	SC05	P
BD436	SC05	P
BD437	SC05	P
BD438	SC05	P
BD643	SC05	P
BD643F	SC05	P
BD644	SC05	P
BD644F	SC05	P
BD645	SC05	P
BD645F	SC05	P
BD646	SC05	P
BD646F	SC05	P
BD647	SC05	P
BD647F	SC05	P
BD648	SC05	P
BD648F	SC05	P
BD649	SC05	P
BD649F	SC05	P
BD650	SC05	P
BD650F	SC05	P
BD651	SC05	P
BD651F	SC05	P
BD652	SC05	P
BD652F	SC05	P
BD675	SC05	P
BD676	SC05	P
BD677	SC05	P
BD678	SC05	P
BD679	SC05	P
BD680	SC05	P
BD681	SC05	P
BD682	SC05	P
BD683	SC05	P

type no.	book	section
BD684	SC05	P
BD719	SC05	P
BD720	SC05	P
BD721	SC05	P
BD722	SC05	P
BD723	SC05	P
BD724	SC05	P
BD725	SC05	P
BD726	SC05	P
BD825	SC05	P
BD826	SC05	P
BD827	SC05	P
BD828	SC05	P
BD829	SC05	P
BD830	SC05	P
BD839	SC05	P
BD840	SC05	P
BD841	SC05	P
BD842	SC05	P
BD843	SC05	P
BD844	SC05	P
BD933	SC05	P
BD933F	SC05	P
BD934	SC05	P
BD934F	SC05	P
BD935	SC05	P
BD935F	SC05	P
BD936	SC05	P
BD936F	SC05	P
BD937	SC05	P
BD937F	SC05	P
BD938	SC05	P
BD938F	SC05	P
BD939	SC05	P
BD939F	SC05	P
BD940	SC05	P
BD940F	SC05	P
BD941	SC05	P
BD941F	SC05	P
BD942	SC05	P
BD942F	SC05	P
BD943	SC05	P
BD943F	SC05	P
BD944	SC05	P
BD944F	SC05	P
BD945	SC05	P
BD945F	SC05	P
BD946	SC05	P
BD946F	SC05	P
BD947	SC05	P
BD947F	SC05	P
BD948	SC05	P
BD948F	SC05	P
BD949	SC05	P
BD949F	SC05	P
BD950	SC05	P
BD950F	SC05	P
BD951	SC05	P
BD951F	SC05	P
BD952	SC05	P
BD952F	SC05	P
BD953	SC05	P
BD953F	SC05	P
BD954	SC05	P
BD954F	SC05	P
BD955	SC05	P
BD955F	SC05	P
BD956	SC05	P
BD956F	SC05	P
BDT29	SC05	P
BDT29F	SC05	P
BDT29A	SC05	P
BDT29AF	SC05	P
BDT29B	SC05	P
BDT29BF	SC05	P
BDT29C	SC05	P
BDT29CF	SC05	P
BDT30	SC05	P
BDT30F	SC05	P
BDT30A	SC05	P
BDT30AF	SC05	P
BDT30B	SC05	P
BDT30BF	SC05	P
BDT30C	SC05	P
BDT30CF	SC05	P
BDT31	SC05	P
BDT31F	SC05	P
BDT31A	SC05	P
BDT31AF	SC05	P
BDT31B	SC05	P
BDT31BF	SC05	P
BDT31C	SC05	P
BDT31CF	SC05	P
BDT31D	SC05	P
BDT31DF	SC05	P
BDT32	SC05	P
BDT32F	SC05	P
BDT32A	SC05	P
BDT32AF	SC05	P
BDT32B	SC05	P
BDT32BF	SC05	P
BDT32C	SC05	P
BDT32CF	SC05	P
BDT32D	SC05	P
BDT32DF	SC05	P
BDT41A	SC05	P
BDT41AF	SC05	P
BDT41B	SC05	P
BDT41BF	SC05	P
BDT41C	SC05	P
BDT41CF	SC05	P
BDT42	SC05	P
BDT42F	SC05	P
BDT42A	SC05	P
BDT42AF	SC05	P
BDT42B	SC05	P
BDT42BF	SC05	P
BDT42C	SC05	P
BDT42CF	SC05	P
BDT60	SC05	P
BDT60F	SC05	P
BDT60A	SC05	P
BDT60AF	SC05	P
BDT60B	SC05	P
BDT60BF	SC05	P
BDT60C	SC05	P
BDT60CF	SC05	P
BDT61	SC05	P
BDT61F	SC05	P
BDT61A	SC05	P
BDT61AF	SC05	P
BDT61B	SC05	P
BDT61BF	SC05	P
BDT61C	SC05	P
BDT61CF	SC05	P

type no.	book	section
BDT62	SC05	P
BDT62F	SC05	P
BDT62A	SC05	P
BDT62AF	SC05	P
BDT62B	SC05	P
BDT62BF	SC05	P
BDT62C	SC05	P
BDT62CF	SC05	P
BDT63	SC05	P
BDT63F	SC05	P
BDT63A	SC05	P
BDT63AF	SC05	P
BDT63B	SC05	P
BDT63BF	SC05	P
BDT63C	SC05	P
BDT63CF	SC05	P
BDT64	SC05	P
BDT64F	SC05	P
BDT64A	SC05	P
BDT64AF	SC05	P
BDT64B	SC05	P
BDT64BF	SC05	P
BDT64C	SC05	P
BDT64CF	SC05	P
BDT65	SC05	P
BDT65F	SC05	P
BDT65A	SC05	P
BDT65AF	SC05	P
BDT65B	SC05	P
BDT65BF	SC05	P
BDT65C	SC05	P
BDT65CF	SC05	P
BDT81	SC05	P
BDT81F	SC05	P
BDT82	SC05	P
BDT82F	SC05	P
BDT83	SC05	P
BDT83F	SC05	P
BDT84	SC05	P
BDT84F	SC05	P
BDT85	SC05	P
BDT85F	SC05	P
BDT86	SC05	P
BDT86F	SC05	P
BDT87	SC05	P
BDT87F	SC05	P
BDT88	SC05	P
BDT88F	SC05	P
BDT91	SC05	P
BDT91F	SC05	P
BDT92	SC05	P
BDT92F	SC05	P
BDT93	SC05	P
BDT93F	SC05	P
BDT94	SC05	P
BDT94F	SC05	P
BDT95	SC05	P
BDT95F	SC05	P
BDT96	SC05	P
BDT96F	SC05	P
BDV64	SC05	P
BDV64A	SC05	P
BDV64B	SC05	P
BDV64C	SC05	P
BDV65	SC05	P
BDV65A	SC05	P
BDV65B	SC05	P
BDV65C	SC05	P
BDV66A	SC05	P
BDV66B	SC05	P
BDV66C	SC05	P
BDV66D	SC05	P
BDV67A	SC05	P
BDV67B	SC05	P
BDV67C	SC05	P
BDV67D	SC05	P
BDV91	SC05	P
BDV92	SC05	P
BDV93	SC05	P
BDV94	SC05	P
BDV95	SC05	P
BDV96	SC05	P
BDX35	SC05	P
BDX36	SC05	P
BDX37	SC05	P
BDX42	SC05	P
BDX43	SC05	P
BDX44	SC05	P
BDX45	SC05	P
BDX46	SC05	P
BDX47	SC05	P
BDX62	SC05	P
BDX62A	SC05	P
BDX62B	SC05	P
BDX62C	SC05	P
BDX63	SC05	P
BDX63A	SC05	P
BDX63B	SC05	P
BDX63C	SC05	P
BDX64	SC05	P
BDX64A	SC05	P
BDX64B	SC05	P
BDX64C	SC05	P
BDX65	SC05	P
BDX65A	SC05	P
BDX65B	SC05	P
BDX65C	SC05	P
BDX66	SC05	P
BDX66A	SC05	P
BDX66B	SC05	P
BDX66C	SC05	P
BDX67	SC05	P
BDX67A	SC05	P
BDX67B	SC05	P
BDX67C	SC05	P
BDX68	SC05	P
BDX68A	SC05	P
BDX68B	SC05	P
BDX68C	SC05	P
BDX69	SC05	P
BDX69A	SC05	P
BDX69B	SC05	P
BDX69C	SC05	P
BDX77	SC05	P
BDX77F	SC05	P
BDX78	SC05	P
BDX78F	SC05	P
BDX91	SC05	P
BDX92	SC05	P
BDX93	SC05	P
BDX94	SC05	P
BDX95	SC05	P
BDX96	SC05	P
BDY90	SC05	P
BDY91	SC05	P

type no.	book	section
BDY92	SC05	P
BF198	SC04	Sm
BF199	SC04	Sm
BF240	SC04	Sm
BF241	SC04	Sm
BF245A	SC07	FET
BF245B	SC07	FET
BF245C	SC07	FET
BF247A	SC07	FET
BF247B	SC07	FET
BF247C	SC07	FET
BF256A	SC07	FET
BF256B	SC07	FET
BF256C	SC07	FET
BF324	SC04	Sm
BF370	SC04	Sm
BF410A	SC07	FET
BF410B	SC07	FET
BF410C	SC07	FET
BF410D	SC07	FET
BF420	SC04	Sm
BF421	SC04	Sm
BF422	SC04	Sm
BF423	SC04	Sm
BF450	SC04	Sm
BF451	SC04	Sm
BF483	SC04	Sm
BF484	SC04	Sm
BF485	SC04	Sm
BF486	SC04	Sm
BF487	SC04	Sm
BF488	SC04	Sm
BF494	SC04	Sm
BF495	SC04	Sm
BF496	SC04	Sm
BF510	SC07/10	FET/Mm
BF511	SC07/10	FET/Mm
BF512	SC07/10	FET/Mm
BF513	SC07/10	FET/Mm
BF550	SC10	Mm
BF550R	SC10	Mm
BF569	SC10	Mm
BF570	SC10	Mm
BF579	SC10	Mm
BF620	SC10	Mm
BF621	SC10	Mm
BF622	SC10	Mm
BF623	SC10	Mm
BF660	SC10	Mm
BF660R	SC10	Mm
BF689K	SC14	WBT
BF720	SC10	Mm
BF721	SC10	Mm
BF722	SC10	Mm
BF723	SC10	Mm
BF763	SC14	WBT
BF820	SC10	Mm
BF821	SC10	Mm
BF822	SC10	Mm
BF823	SC10	Mm
BF824	SC10	Mm
BF840	SC10	Mm
BF841	SC10	Mm
BF926	SC04	Sm
BF936	SC04	Sm
BF939	SC04	Sm
BF960	SC07	FET
BF964S	SC07	FET
BF965	SC07	FET
BF966S	SC07	FET
BF967	SC04	Sm
BF970	SC04	Sm
BF970A	SC04	Sm
BF979	SC04	Sm
BF980	SC07	FET
BF980A	SC07	FET
BF981	SC07	FET
BF982	SC07	FET
BF989	SC07/10	FET/Mm
BF990A	SC07/10	FET/Mm
BF990AR	SC07/10	FET/Mm
BF991	SC07/10	FET/Mm
BF992	SC07/10	FET/Mm
BF992R	SC07/10	FET/Mm
BF994S	SC07/10	FET/Mm
BF994SR	SC07/10	FET/Mm
BF996S	SC07/10	FET/Mm
BF996SR	SC07/10	FET/Mm
BF997	SC07/10	FET/Mm
BFG17A	SC14	WBT
BFG23	SC14	WBT
BFG32	SC14	WBT
BFG33	SC14	WBT
BFG34	SC14	WBT
BFG35	SC14/10	WBT/Mm
BFG51	SC14	WBT
BFG65	SC14	WBT
BFG67	SC14/10	WBT/Mm
BFG90A	SC14	WBT
BFG91A	SC14	WBT
BFG92A	SC14	WBT
BFG93A	SC14	WBT
BFG96	SC14	WBT
BFG97	SC14/10	WBT/Mm
BFG134	SC14	WBT
BFG135	SC14/10	WBT/Mm
BFG195	SC14	WBT
BFG197	SC14	WBT
BFG198	SC14/10	WBT/Mm
BFP90A	SC14	WBT
BFP91A	SC14	WBT
BFP96	SC14	WBT
BFQ10	SC07	FET
BFQ11	SC07	FET
BFQ12	SC07	FET
BFQ13	SC07	FET
BFQ14	SC07	FET
BFQ15	SC07	FET
BFQ16	SC07	FET
BFQ17	SC14/10	WBT/Mm
BFQ18A	SC14/10	WBT/Mm
BFQ19	SC14/10	WBT/Mm
BFQ22S	SC14	WBT
BFQ23	SC14	WBT
BFQ23C	SC14	WBT
BFQ24	SC14	WBT
BFQ32	SC14	WBT
BFQ32C	SC14	WBT
BFQ32M	SC14	WBT
BFQ32S	SC14	WBT
BFQ33	SC14	WBT
BFQ33C	SC14	WBT
BFQ34	SC14	WBT
BFQ34T	SC14	WBT
BFQ42	SC08	RFP

type no.	book	section
BFQ43	SC08	RFP
BFQ43S	SC08	RFP
BFQ51	SC14	WBT
BFQ51C	SC14	WBT
BFQ52	SC14	WBT
BFQ53	SC14	WBT
BFQ54	SC14	WBT
BFQ54T	SC14	WBT
BFQ63	SC14	WBT
BFQ65	SC14	WBT
BFQ66	SC14	WBT
BFQ67	SC14/10	WBT/Mm
BFQ68	SC14	WBT
BFQ135	SC14	WBT
BFQ136	SC14	WBT
BFQ149	SC14	WBT
BFQ162	SC14	WBT
BFQ163	SC14	WBT
BFQ232	SC14	WBT
BFQ233	SC14	WBT
BFQ234	SC14	WBT
BFQ252	SC14	WBT
BFQ253	SC14	WBT
BFQ254	SC14	WBT
BFQ262	SC14	WBT
BFQ263	SC14	WBT
BFQ268	SC14	WBT
BFR29	SC07	FET
BFR30	SC07/10	FET/Mm
BFR31	SC07/10	FET/Mm
BFR49	SC14	WBT
BFR53	SC14/10	WBT/Mm
BFR54	SC04	Sm
BFR64	SC14	WBT
BFR65	SC14	WBT
BFR84	SC07	FET
BFR90	SC14	WBT
BFR90A	SC14	WBT
BFR91	SC14	WBT
BFR91A	SC14	WBT
BFR92	SC14/10	WBT/Mm
BFR92A	SC14/10	WBT/Mm
BFR93	SC14/10	WBT/Mm
BFR93A	SC14/10	WBT/Mm
BFR94	SC14	WBT
BFR95	SC14	WBT
BFR96	SC14	WBT
BFR96S	SC14	WBT
BFR101A	SC07/10	FET/Mm
BFR101B	SC07/10	FET/Mm
BFR106	SC14	WBT
BFR134	SC14	WBT
BFS17	SC14/10	WBT
BFS17A	SC14	WBT
BFS18	SC10	Mm
BFS18R	SC10	Mm
BFS19	SC10	Mm
BFS19R	SC10	Mm
BFS20	SC10	Mm
BFS20R	SC10	Mm
BFS21	SC07	FET
BFS21A	SC07	FET
BFS22A	SC08	RFP
BFS23A	SC08	RFP
BFT24	SC14	WBT
BFT25	SC14/10	WBT/Mm
BFT44	SC04	Sm
BFT45	SC04	Sm
BFT46	SC07/10	FET/Mm
BFT92	SC14/10	WBT/Mm
BFT93	SC14/10	WBT/Mm
BFW10	SC07	FET
BFW11	SC07	FET
BFW12	SC07	FET
BFW13	SC07	FET
BFW16A	SC14	WBT
BFW17A	SC14	WBT
BFW30	SC14	WBT
BFW61	SC07	FET
BFW92	SC14	WBT
BFW92A	SC14	WBT
BFW93	SC14	WBT
BFX29	SC04	Sm
BFX30	SC04	Sm
BFX34	SC04	Sm
BFX84	SC04	Sm
BFX85	SC04	Sm
BFX87	SC04	Sm
BFX88	SC04	Sm
BFX89	SC14	WBT
BFY50	SC04	Sm
BFY51	SC04	Sm
BFY52	SC04	Sm
BFY55	SC04	Sm
BFY90	SC14	WBT
BG2000	SC01	RT
BG2097	SC01	RT
BGD102	SC14	WBM
BGD102E	SC14	WBM
BGD104	SC14	WBM
BGD104E	SC14	WBM
BGD502	SC14	WBM
BGD504	SC14	WBM
BGE88	SC14	WBM
BGE88/01	SC14	WBM
BGE85A	SC14	WBM
BGX885	SC14	WBM
BGY22	SC09	RFP
BGY22A	SC09	RFP
BGY23	SC09	RFP
BGY23A	SC09	RFP
BGY32	SC09	RFP
BGY33	SC09	RFP
BGY35	SC09	RFP
BGY36	SC09	RFP
BGY40A	SC09	RFP
BGY40B	SC09	RFP
BGY41A	SC09	RFP
BGY41B	SC09	RFP
BGY43	SC09	RFP
BGY45A	SC09	RFP
BGY45B	SC09	RFP
BGY45C	SC09	RFP
BGY46A	SC09	RFP
BGY46B	SC09	RFP
BGY47A	SC09	RFP
BGY47F	SC09	RFP
BGY48A	SC09	RFP
BGY48B	SC09	RFP
BGY48C	SC09	RFP
BGY49A	SC09	RFP
BGY49B	SC09	RFP
BGY50	SC14	WBM
BGY51	SC14	WBM
BGY52	SC14	WBM

type no.	book	section
BGY53	SC14	WBM
BGY54	SC14	WBM
BGY55	SC14	WBM
BGY56	SC14	WBM
BGY57	SC14	WBM
BGY58	SC14	WBM
BGY58A	SC14	WBM
BGY59	SC14	WBM
BGY60	SC14	WBM
BGY61	SC14	WBM
BGY65	SC14	WBM
BGY67	SC14	WBM
BGY67A	SC14	WBM
BGY80	SC14	WBM
BGY81	SC14	WBM
BGY84	SC14	WBM
BGY84A	SC14	WBM
BGY84H	SC14	WBM
BGY85	SC14	WBM
BGY85A	SC14	WBM
BGY85H	SC14	WBM
BGY86	SC14	WBM
BGY87	SC14	WBM
BGY88	SC14	WBM
BGY89	SC14	WBM
BGY90A	SC09	RFP
BGY90B	SC09	RFP
BGY91A	SC09	RFP
BGY91B	SC09	RFP
BGY93A	SC09	RFP
BGY93B	SC09	RFP
BGY93C	SC09	RFP
BGY94A	SC09	RFP
BGY94B	SC09	RFP
BGY94C	SC09	RFP
BGY95A	SC09	RFP
BGY95B	SC09	RFP
BGY96A	SC09	RFP
BGY96B	SC09	RFP
BGY110A	SC09	RFP
BGY110B	SC09	RFP
BGY580	SC14	WBM
BGY581	SC14	WBM
BGY584	SC14	WBM
BGY584A	SC14	WBM
BGY585	SC14	WBM
BGY585A	SC14	WBM
BGY586	SC14	WBM
BGY587	SC14	WBM
BGY588	SC14	WBM
BLF145	SC08	RFP/FET
BLF147	SC08	RFP/FET
BLF175	SC08	RFP/FET
BLF177	SC08	RFP/FET
BLF221	SC08	RFP/FET
BLF241	SC08	RFP/FET
BLF242	SC08	RFP/FET
BLF244	SC08	RFP/FET
BLF245	SC08	RFP/FET
BLF246	SC08	RFP/FET
BLF278	SC08	RFP/FET
BLF368	SC08	RFP/FET
BLF378	SC08	RFP/FET
BLF521	SC08	RFP/FET
BLF522	SC08	RFP/FET
BLF543	SC08	RFP/FET
BLF544	SC08	RFP/FET
BLF545	SC08	RFP/FET
BLF547	SC08	RFP/FET
BLF548	SC08	RFP/FET
BLT90/SL	SC08	RFP
BLT91/SL	SC08	RFP
BLT92/SL	SC08	RFP
BLT93/SL	SC08	RFP
BLU20/12	SC08	RFP
BLU30/12	SC08	RFP
BLU30/28	SC08	RFP
BLU45/12	SC08	RFP
BLU50	SC08	RFP
BLU51	SC08	RFP
BLU52	SC08	RFP
BLU53	SC08	RFP
BLU60/12	SC08	RFP
BLU60/28	SC08	RFP
BLU97	SC08	RFP
BLU98	SC08	RFP
BLU99	SC08	RFP
BLV10	SC08	RFP
BLV11	SC08	RFP
BLV20	SC08	RFP
BLV21	SC08	RFP
BLV25	SC08	RFP
BLV30	SC08	RFP
BLV30/12	SC08	RFP
BLV31	SC08	RFP
BLV32F	SC08	RFP
BLV33	SC08	RFP
BLV33F	SC08	RFP
BLV36	SC08	RFP
BLV37	SC08	RFP
BLV38	SC08	RFP
BLV45/12	SC08	RFP
BLV57	SC08	RFP
BLV59	SC08	RFP
BLV75/12	SC08	RFP
BLV80/28	SC08	RFP
BLV90	SC08	RFP
BLV90/SL	SC08	RFP
BLV91	SC08	RFP
BLV91/SL	SC08	RFP
BLV92	SC08	RFP
BLV93	SC08	RFP
BLV94	SC08	RFP
BLV95	SC08	RFP
BLV97	SC08	RFP
BLV98	SC08	RFP
BLV99	SC08	RFP
BLW29	SC08	RFP
BLW31	SC08	RFP
BLW32	SC08	RFP
BLW33	SC08	RFP
BLW34	SC08	RFP
BLW50F	SC08	RFP
BLW60	SC08	RFP
BLW60C	SC08	RFP
BLW76	SC08	RFP
BLW77	SC08	RFP
BLW78	SC08	RFP
BLW79	SC08	RFP
BLW80	SC08	RFP
BLW81	SC08	RFP
BLW83	SC08	RFP
BLW84	SC08	RFP
BLW85	SC08	RFP
BLW86	SC08	RFP

type no.	book	section
BLW87	SC08	RFP
BLW89	SC08	RFP
BLW90	SC08	RFP
BLW91	SC08	RFP
BLW95	SC08	RFP
BLW96	SC08	RFP
BLW97	SC08	RFP
BLW98	SC08	RFP
BLW99	SC08	RFP
BLX13	SC08	RFP
BLX13C	SC08	RFP
BLX14	SC08	RFP
BLX15	SC08	RFP
BLX39	SC08	RFP
BLX65	SC08	RFP
BLX65E	SC08	RFP
BLX65ES	SC08	RFP
BLX67	SC08	RFP
BLX68	SC08	RFP
BLX69A	SC08	RFP
BLX91A	SC08	RFP
BLX91CB	SC08	RFP
BLX92A	SC08	RFP
BLX93A	SC08	RFP
BLX94A	SC08	RFP
BLX94C	SC08	RFP
BLX95	SC08	RFP
BLX96	SC08	RFP
BLX97	SC08	RFP
BLX98	SC08	RFP
BLY87A	SC08	RFP
BLY87C	SC08	RFP
BLY88A	SC08	RFP
BLY88C	SC08	RFP
BLY89A	SC08	RFP
BLY89C	SC08	RFP
BLY90	SC08	RFP
BLY91A	SC08	RFP
BLY91C	SC08	RFP
BLY92A	SC08	RFP
BLY92C	SC08	RFP
BLY93A	SC08	RFP
BLY93C	SC08	RFP
BLY94	SC08	RFP
BR100/03	S2b	Th
BR101	SC04	Sm
BR210*	S2a	Th
BR216*	S2a	Th
BR220*	S2a	Th
BRY39	SC04	Sm
BRY56	SC04	Sm
BRY61	SC10	Mm
BRY62	SC10	Mm
BS107	SC07	FET
BS107A	SC07	FET
BS170	SC07	FET
BS250	SC07	FET
BSD10	SC07	FET
BSD12	SC07	FET
BSD20	SC07/10	FET/m
BSD22	SC07/10	FET/M
BSD212	SC07	FET
BSD213	SC07	FET
BSD214	SC07	FET
BSD215	SC07	FET
BSJ111	SC07	FET
BSJ112	SC07	FET
BSJ113	SC07	FET
BSJ174	SC07	FET
BSJ175	SC07	FET
BSJ176	SC07	FET
BSJ177	SC07	FET
BSN205	SC07	FET
BSN205A	SC07	FET
BSN254	SC07	FET
BSN254A	SC07	FET
BSP15	SC10	Mm
BSP16	SC10	Mm
BSP19	SC10	Mm
BSP20	SC10	Mm
BSP30	SC10	Mm
BSP31	SC10	Mm
BSP32	SC10	Mm
BSP33	SC10	Mm
BSP40	SC10	Mm
BSP41	SC10	Mm
BSP42	SC10	Mm
BSP43	SC10	Mm
BSP50	SC10	Mm
BSP51	SC10	Mm
BSP52	SC10	Mm
BSP60	SC10	Mm
BSP61	SC10	Mm
BSP62	SC10	Mm
BSP204	SC07	FET
BSP204A	SC07	FET
BSR12	SC10	Mm
BSR12R	SC10	Mm
BSR13	SC10	Mm
BSR13R	SC10	Mm
BSR14	SC10	Mm
BSR14R	SC10	Mm
BSR15	SC10	Mm
BSR15R	SC10	Mm
BSR16	SC10	Mm
BSR16R	SC10	Mm
BSR17	SC10	Mm
BSR17R	SC10	Mm
BSR17A	SC10	Mm
BSR17AR	SC10	Mm
BSR18	SC10	Mm
BSR18R	SC10	Mm
BSR18A	SC10	Mm
BSR18AR	SC10	Mm
BSR19	SC10	Mm
BSR19A	SC10	Mm
BSR20	SC10	Mm
BSR20A	SC10	Mm
BSR30	SC10	Mm
BSR31	SC10	Mm
BSR32	SC10	Mm
BSR33	SC10	Mm
BSR40	SC10	Mm
BSR41	SC10	Mm
BSR42	SC10	Mm
BSR43	SC10	Mm
BSR50	SC04	Sm
BSR51	SC04	Sm
BSR52	SC04	Sm
BSR56	SC07/10	FET/Mm
BSR57	SC07/10	FET/Mm
BSR58	SC07/10	FET/Mm
BSR60	SC04	Sm
BSR61	SC04	Sm
BSR62	SC04	Sm

type no.	book	section
BSR111	SC07/10	FET/Mm
BSR112	SC07/10	FET/Mm
BSR113	SC07/10	FET/Mm
BSR174	SC07/10	FET/Mm
BSR175	SC07/10	FET/Mm
BSR176	SC07/10	FET/Mm
BSR177	SC07/10	FET/Mm
BSS38	SC04	Sm
BSS50	SC04	Sm
BSS51	SC04	Sm
BSS52	SC04	Sm
BSS60	SC04	Sm
BSS61	SC04	Sm
BSS62	SC04	Sm
BSS63	SC10	Mm
BSS63R	SC10	Mm
BSS64	SC10	Mm
BSS64R	SC10	Mm
BSS68	SC04	Sm
BSS83	SC07/10	FET/Mm
BSS87	SC07	FET
BSS89	SC07	FET
BSS91	SC07	FET
BSS92	SC07	FET
BST15	SC10	Mm
BST16	SC10	Mm
BST39	SC10	Mm
BST40	SC10	Mm
BST50	SC10	Mm
BST51	SC10	Mm
BST52	SC10	Mm
BST60	SC10	Mm
BST61	SC10	Mm
BST62	SC10	Mm
BST70A	SC07	FET
BST72A	SC07	FET
BST74A	SC07	FET
BST76A	SC07	FET
BST78	SC07	FET
BST80	SC07/10	FET/Mm
BST82	SC07/10	FET/Mm
BST84	SC07/10	FET/Mm
BST86	SC07/10	FET/Mm
BST95	SC07	FET
BST97	SC07	FET
BST100	SC07	FET
BST110	SC07	FET
BST120	SC07/10	FET/Mm
BST122	SC07/10	FET/Mm
BSV15	SC04	Sm
BSV16	SC04	Sm
BSV17	SC04	Sm
BSV52	SC10	Mm
BSV52R	SC10	Mm
BSV64	SC04	Sm
BSV78	SC07	FET
BSV79	SC07	FET
BSV80	SC07	FET
BSV81	SC07	FET
BSW66A	SC04	Sm
BSW67A	SC04	Sm
BSW68A	SC04	Sm
BSX20	SC04	Sm
BSX32	SC04	Sm
BSX45	SC04	Sm
BSX46	SC04	Sm
BSX47	SC04	Sm
BSX59	SC04	Sm
BSX60	SC04	Sm
BSX61	SC04	Sm
BSY95A	SC04	Sm
BT136*	S2b	Tri
BT136F*	S2b	Tri
BT137*	S2b	Tri
BT137F*	S2b	Tri
BT138*	S2b	Tri
BT138F*	S2b	Tri
BT139*	S2b	Tri
BT139F*	S2b	Tri
BT145*	S2b	Tri
BT149*	S2b	Th
BT150	S2b	Th
BT151*	S2b	Th
BT151F*	S2b	Th
BT152*	S2b	Th
BT153	S2b	Th
BT157*	S2b	Th
BT169*	S2b	Th
BTA140*	S2b	Tri
BTR59*	S2b	Tri
BTS59*	S2b	Tri
BTV58*	S2b	Th
BTV59*	S2b	Th
BTV59D*	S2b	Th
BTV60*	S2b	Th
BTV60D*	S2b	Th
BTV70*	S2b	Th
BTV70D*	S2b	Th
BTW23*	S2b	Th
BTW38*	S2b	Th
BTW40*	S2b	Th
BTW42*	S2b	Th
BTW43*	S2b	Tri
BTW45*	S2b	Th
BTW58*	S2b	Th
BTW62*	S2b	Th
BTW62D*	S2b	Th
BTW63*	S2b	Th
BTY79*	S2b	Th
BTY91*	S2b	Th
BU306	SC06	SP
BU306F	SC06	SP
BU505	SC06	SP
BU506	SC06	SP
BU506D	SC06	SP
BU508A	SC06	SP
BU508D	SC06	SP
BU705	SC06	SP
BU706	SC06	SP
BU706D	SC06	SP
BU806	SC06	SP
BU807	SC06	SP
BU808	SC06	SP
BU824	SC06	SP
BU826	SC06	SP
BUP22*	SC06	SP
BUP23*	SC06	SP
BUS11	SC06	SP
BUS11A	SC06	SP
BUS12	SC06	SP
BUS12A	SC06	SP
BUS13	SC06	SP
BUS13A	SC06	SP
BUS14	SC06	SP
BUS14A	SC06	SP

type no.	book	section
BUS21*	SC06	SP
BUS22*	SC06	SP
BUS23*	SC06	SP
BUS24*	SC06	SP
BUS131*	SC06	SP
BUS132*	SC06	SP
BUS133*	SC06	SP
BUT11	SC06	SP
BUT11A	SC06	SP
BUT11F	SC06	SP
BUT11AF	SC06	SP
BUT12	SC06	SP
BUT12A	SC06	SP
BUT12F	SC06	SP
BUT12AF	SC06	SP
BUT18	SC06	SP
BUT18A	SC06	SP
BUT18F	SC06	SP
BUT18AF	SC06	SP
BUT21B	SC06	SP
BUT21C	SC06	SP
BUT21BF	SC06	SP
BUT21CF	SC06	SP
BUT22B	SC06	SP
BUT22C	SC06	SP
BUT22BF	SC06	SP
BUT22CF	SC06	SP
BUT131	SC06	SP
BUV26	SC06	SP
BUV26A	SC06	SP
BUV26F	SC06	SP
BUV26AF	SC06	SP
BUV27	SC06	SP
BUV27A	SC06	SP
BUV27F	SC06	SP
BUV27AF	SC06	SP
BUV28	SC06	SP
BUV28A	SC06	SP
BUV28F	SC06	SP
BUV28AF	SC06	SP
BUV47	SC06	SP
BUV47A	SC06	SP
BUV48	SC06	SP
BUV48A	SC06	SP
BUV82	SC06	SP
BUV83	SC06	SP
BUV89	SC06	SP
BUV90	SC06	SP
BUV90F	SC06	SP
BUV98 (V)	SC06	SP
BUV98A	SC06	SP
BUV298 (V)	SC06	SP
BUV298A	SC06	SP
BUW11	SC06	SP
BUW11A	SC06	SP
BUW12	SC06	SP
BUW12A	SC06	SP
BUW12F	SC06	SP
BUW12AF	SC06	SP
BUW13	SC06	SP
BUW13A	SC06	SP
BUW13F	SC06	SP
BUW13AF	SC06	SP
BUW84	SC06	SP
BUW85	SC06	SP
BUW86	SC06	SP
BUW87	SC06	SP
BUW87A	SC06	SP
BUW131*	SC06	SP
BUW132*	SC06	SP
BUW133*	SC06	SP
BUX46	SC06	SP
BUX46A	SC06	SP
BUX47	SC06	SP
BUX47A	SC06	SP
BUX48	SC06	SP
BUX48A	SC06	SP
BUX84	SC06	SP
BUX84F	SC06	SP
BUX85	SC06	SP
BUX85F	SC06	SP
BUX86	SC06	SP
BUX87	SC06	SP
BUX88	SC06	SP
BUX98	SC06	SP
BUX98A	SC06	SP
BUX99	SC06	SP
BUY89	SC06	SP
BUZ10	S9	PM
BUZ11	S9	PM
BUZ11A	S9	PM
BUZ14	S9	PM
BUZ15	S9	PM
BUZ20	S9	PM
BUZ21	S9	PM
BUZ23	S9	PM
BUZ24	S9	PM
BUZ25	S9	PM
BUZ31	S9	PM
BUZ32	S9	PM
BUZ34	S9	PM
BUZ35	S9	PM
BUZ36	S9	PM
BUZ41A	S9	PM
BUZ42	S9	PM
BUZ45	S9	PM
BUZ45A	S9	PM
BUZ45B	S9	PM
BUZ50A	S9	PM
BUZ50B	S9	PM
BUZ50C	S9	PM
BUZ53A	S9	PM
BUZ54	S9	PM
BUZ54A	S9	PM
BUZ60	S9	PM
BUZ63	S9	PM
BUZ64	S9	PM
BUZ71	S9	PM
BUZ71A	S9	PM
BUZ72	S9	PM
BUZ72A	S9	PM
BUZ73	S9	PM
BUZ73A	S9	PM
BUZ74	S9	PM
BUZ74A	S9	PM
BUZ76	S9	PM
BUZ76A	S9	PM
BUZ78	S9	PM
BUZ80	S9	PM
BUZ80A	S9	PM
BUZ83	S9	PM
BUZ83A	S9	PM
BUZ84	S9	PM
BUZ84A	S9	PM
BUZ90	S9	PM

type no.	book	section
BUZ90A	S9	PM
BUZ94	S9	PM
BUZ211	S9	PM
BUZ307	S9	PM
BUZ308	S9	PM
BUZ310	S9	PM
BUZ311	S9	PM
BUZ326	S9	PM
BUZ330	S9	PM
BUZ331	S9	PM
BUZ347	S9	PM
BUZ348	S9	PM
BUZ349	S9	PM
BUZ350	S9	PM
BUZ351	S9	PM
BUZ355	S9	PM
BUZ356	S9	PM
BUZ357	S9	PM
BUZ358	S9	PM
BUZ384	S9	PM
BUZ385	S9	PM
BY224*	S2a	R
BY225*	S2a	R
BY228	SC01	R
BY229*	S2a	R
BY229F*	S2a	R
BY249*	S2a	R
BY260*	S2a	R
BY261*	S2a	R
BY328	SC01	SD
BY329*	S2a	R
BY359*	S2a	R
BY438	SC01	R
BY448	SC01	R
BY458	SC01	R
BY505	SC01	R
BY509	SC01	R
BY527	SC01	R
BY584	SC01	R
BY588	SC01	R
BY609	SC01	R
BY610	SC01	R
BY614	SC01	R
BY619	SC01	R
BY620	SC01	R
BY627	SC01	R
BY705	SC01	R
BY706	SC01	R
BY707	SC01	R
BY708	SC01	R
BY709	SC01	R
BY710	SC01	R
BY711	SC01	R
BY712	SC01	R
BY713	SC01	R
BY714	SC01	R
BY715	SC01	R
BY716	SC01	R
BY717	SC01	R
BY718	SC01	R
BY719	SC01	R
BY720	SC01	R
BY721	SC01	R
BY722	SC01	R
BY723	SC01	R
BY724	SC01	R
BYD11*	SC01	R
BYD13*	SC01	R
BYD14*	SC01	R
BYD17*	SC01/10	R/Mn
BYD31*	SC01	R
BYD33*	SC01	R
BYD34*	SC01	R
BYD37*	SC01/10	R/Mn
BYD73*	SC01	R
BYD74*	SC01	R
BYD77*	SC01	R
BYM26*	SC01	R
BYM36*	SC01	R
BYM56*	SC01	R
BYP21*	S2a	R
BYP22*	S2a	R
BYP59*	S2a	R
BYQ27*	SC01	R
BYQ28*	S2a	R
BYR29*	S2a	R
BYR29F*	S2a	R
BYR30*	SC01	R
BYR79*	SC01	R
BYT28*	S2a	R
BYT79*	S2a	R
BYT230PIV	SC01	R
BYV10*	SC01	R
BYV18*	S2a	R
BYV19*	S2a	R
BYV20*	S2a	R
BYV21*	S2a	R
BYV22*	S2a	R
BYV23*	S2a	R
BYV24*	S2a	R
BYV26*	SC01/S2a	R
BYV27*	SC01/S2a	R
BYV28*	SC01/S2a	R
BYV29*	S2a	R
BYV29F*	S2a	R
BYV30*	S2a	R
BYV31*	S2a	R
BYV32*	S2a	R
BYV32F*	S2a	R
BYV33*	S2a	R
BYV33F*	S2a	R
BYV34*	S2a	R
BYV36*	SC01	R
BYV39*	S2a	R
BYV42*	S2a	R
BYV43*	S2a	R
BYV43F*	S2a	R
BYV44*	S2a	R
BYV54V	SC01	R
BYV60*	S2a	R
BYV72*	S2a	R
BYV73*	S2a	R
BYV74*	S2a	R
BYV79*	S2a	R
BYV92*	S2a	R
BYV95A	SC01	R
BYV95B	SC01	R
BYV95C	SC01	R
BYV96D	SC01	R
BYV96E	SC01	R
BYW25*	S2a	R
BYW29*	S2a	R
BYW29F*	S2a	R
BYW30*	S2a	R
BYW31*	S2a	R

type no.	book	section
BYW54	SC01	R
BYW55	SC01	R
BYW56	SC01	R
BYW92*	S2a	R
BYW93*	S2a	R
BYW95A	SC01	R
BYW95B	SC01	R
BYW95C	SC01	R
BYW96D	SC01	R
BYW96E	SC01	R
BYX10G	SC01	R
BYX25*	S2a	R
BYX30*	S2a	R
BYX32*	S2a	R
BYX38*	S2a	R
BYX39*	S2a	R
BYX42*	S2a	R
BYX46*	S2a	R
BYX50*	S2a	R
BYX52*	S2a	R
BYX56*	S2a	R
BYX90G	SC01	R
BYX96*	S2a	R
BYX97*	S2a	R
BYX98*	S2a	R
BYX99*	S2a	R
BZD23	SC01	Vrg
BZD27	SC01/10	Vrg/Mm
BZT03	SC01	Vrg
BZV10	SC01	Vrf
BZV11	SC01	Vrf
BZV12	SC01	Vrf
BZV13	SC01	Vrf
BZV14	SC01	Vrf
BZV37	SC01	Vrf
BZV49*	SC01/10	Vrg/Mm
BZV55*	SC10	Mm
BZV60	SC01	Vrg
BZV80	SC01	Vrf
BZV81	SC01	Vrf
BZV85*	SC01	Vrg
BZV86	SC01	SD
BZW03*	SC01	Vrg
BZW14	SC01	Vrg
BZW86*	S2a	TS
BZX55*	SC01	Vrg
BZX70*	S2a	Vrg
BZX75*	SC01	Vrg
BZX79*	SC01	Vrg
BZX84*	SC01/10	Vrg/Mm
BZY91*	S2a	Vrg
BZY93*	S2a	Vrg
CNG35	SC12	PhC
CNG36	SC12	PhC
CNR36	SC12	PhC
CNX21	SC12	PhC
CNX35	SC12	PhC
CNX35U	SC12	PhC
CNX36	SC12	PhC
CNX36U	SC12	PhC
CNX38	SC12	PhC
CNX38U	SC12	PhC
CNX39	SC12	PhC
CNX39U	SC12	PhC
CNX44	SC12	PhC
CNX44A	SC12	PhC
CNX46	SC12	PhC
CNX48	SC12	PhC
CNX48U	SC12	PhC
CNX72	SC12	PhC
CNX82	SC12	PhC
CNX83	SC12	PhC
CNX91	SC12	PhC
CNX92	SC12	PhC
CNY17-1	SC12	PhC
CNY17-2	SC12	PhC
CNY17-3	SC12	PhC
CNY50	SC12	PhC
CNY57	SC12	PhC
CNY57A	SC12	PhC
CNY57AU	SC12	PhC
CNY57U	SC12	PhC
CNY62	SC12	PhC
CNY63	SC12	PhC
CQW58A	S8a	I
CQW89A	S8a	I
CQW89B	S8a	I
CQY58A	S8a	I
CQY89A	S8a	I
CQY89F	S8a	I
ESM3045A(V)	SC06	SP
ESM3045D(V)	SC06	SP
ESM4045A(V)	SC06	SP
ESM4045D(V)	SC06	SP
ESM5045D(V)	SC06	SP
ESM6045A(V)	SC06	SP
ESM6045D(V)	SC06	SP
Fresnel-lens	SC12	A
H11A1	SC12	PhC
H11A2	SC12	PhC
H11A3	SC12	PhC
H11A4	SC12	PhC
H11A5	SC12	PhC
H11B1	SC12	PhC
H11B2	SC12	PhC
H11B3	SC12	PhC
H11B255	SC12	PhC
JA100	SC04	Sm
JA101	SC04	Sm
JC500	SC04	Sm
JC501	SC04	Sm
JC546	SC04	Sm
JC547	SC04	Sm
JC548	SC04	Sm
JC556	SC04	Sm
JC557	SC04	Sm
JC558	SC04	Sm
KMZ10A	SC17	SEN
KMZ10B	SC17	SEN
KMZ10C	SC17	SEN
KP100A	SC17	SEN
KP101A	SC17	SEN
KPZ20G	SC17	SEN
KPZ21G	SC17	SEN
KTY81-100*	SC17	SEN
KTY81-200*	SC17	SEN
KTY83-100*	SC17	SEN
KTY84-100*	SC17	SEN
KTY85-100*	SC10/17	SEN
LAE2001R	SC15	M
LAE4000Q	SC15	M
LAE4001R	SC15	M
LAE4002S	SC15	M
LAE6000Q	SC15	M
LBE1004R	SC15	M

type no.	book	section
LBE1010R	SC15	M
LBE2003S	SC15	M
LBE2005Q	SC15	M
LBE2008T	SC15	M
LBE2009S	SC15	M
LCE1004R	SC15	M
LCE1010R	SC15	M
LCE2003S	SC15	M
LCE2005Q	SC15	M
LCE2008T	SC15	M
LCE2009S	SC15	M
LJE42002T	SC15	M
LKE1004R	SC15	M
LKE2002T	SC15	M
LKE2004T	SC15	M
LKE2015T	SC15	M
LKE21004R	SC15	M
LKE21015T	SC15	M
LKE21050T	SC15	M
LKE27010R	SC15	M
LKE27025R	SC15	M
LKE32002T	SC15	M
LKE32004T	SC15	M
LTE21009R	SC15	M
LTE21015R	SC15	M
LTE21025R	SC15	M
LTE4002S	SC15	M
LTE42005S	SC15	M
LTE42008R	SC15	M
LTE42012R	SC15	M
LUE2003S	SC15	M
LUE2009S	SC15	M
LV172E50R	SC15	M
LV2024E45R	SC15	M
LV2327E40R	SC15	M
LV2931E50S	SC15	M
LV3742E16R	SC15	M
LV3742E24R	SC15	M
LVE21050R	SC15	M
LWE2015R	SC15	M
LWE2025R	SC15	M
LZ1418E100R	SC15	M
MCA230	SC12	PhC
MCA231	SC12	PhC
MCA255	SC12	PhC
MCT2	SC12	PhC
MCT26	SC12	PhC
MJE13004	SC06	SP
MJE13005	SC06	SP
MJE13006	SC06	SP
MJE13007	SC06	SP
MJE13008	SC06	SP
MJE13009	SC06	SP
MKB12040WS	SC15	M
MKB12100WS	SC15	M
MKB12140W	SC15	M
MO6075B200Z	SC15	M
MO6075B400Z	SC15	M
MPS3702	SC04	Sm
MPS3703	SC04	Sm
MPS3704	SC04	Sm
MPS3705	SC04	Sm
MPS3706	SC04	Sm
MPS6513	SC04	Sm
MPS6514	SC04	Sm
MPS6515	SC04	Sm
MPS6517	SC04	Sm
MPS6518	SC04	Sm
MPS6519	SC04	Sm
MPS6520	SC04	Sm
MPS6521	SC04	Sm
MPS6522	SC04	Sm
MPS6523	SC04	Sm
MPSA05	SC04	Sm
MPSA06	SC04	Sm
MPSA13	SC04	Sm
MPSA14	SC04	Sm
MPSA25	SC04	Sm
MPSA26	SC04	Sm
MPSA27	SC04	Sm
MPSA42	SC04	Sm
MPSA43	SC04	Sm
MPSA55	SC04	Sm
MPSA56	SC04	Sm
MPSA63	SC04	Sm
MPSA64	SC04	Sm
MPSA92	SC04	Sm
MPSA93	SC04	Sm
MRB11080Y	SC15	M
MRB11175Y	SC15	M
MRB11350Y	SC15	M
MRB12175YR	SC15	M
MRB12350YR	SC15	M
MS1011B700Y	SC15	M
MS6075B800Z	SC15	M
MSB11900Y	SC15	M
MSB12900Y	SC15	M
MZ0912B75Y	SC15	M
MZ0912B150Y	SC15	M
OM200/52	SC04	-
OM286	SC17	SEN
OM286M	SC17	SEN
OM287	SC17	SEN
OM287M	SC17	SEN
OM320	SC14	WBM
OM321	SC14	WBM
OM322	SC14	WBM
OM323	SC14	WBM
OM323A	SC14	WBM
OM335	SC14	WBM
OM336	SC14	WBM
OM337	SC14	WBM
OM337A	SC14	WBM
OM339	SC14	WBM
OM345	SC14	WBM
OM350	SC14	WBM
OM360	SC14	WBM
OM361	SC14	WBM
OM370	SC14	WBM
OM386B	SC17	SEN
OM386M	SC17	SEN
OM387B	SC17	SEN
OM387M	SC17	SEN
OM388B	SC17	SEN
OM389B	SC17	SEN
OM931	SC05	P
OM961	SC05	P
OSB9115	S2a	St
OSB9215	S2a	St
OSB9415	S2a	St
OSM9115	S2a	St
OSM9215	S2a	St
OSM9415	S2a	St
OSM9510	S2a	St
OSM9511	S2a	St

type no.	book	section
OSM9512	S2a	St
OSS9115	S2a	St
OSS9215	S2a	St
OSS9415	S2a	St
P2105	SC17	SEN
PDE1001U	SC15	M
PDE1003U	SC15	M
PDE1005U	SC15	M
PDE1010U	SC15	M
PEE1001U	SC15	M
PEE1003U	SC15	M
PEE1005U	SC15	M
PEE1010U	SC15	M
PH2222/A	SC04	Sm
PH2369	SC04	Sm
PH2907	SC04	Sm
PH2907A	SC04	Sm
PH5415	SC04	Sm
PH5416	SC04	Sm
PH6659	SC07	FET
PH6660	SC07	FET
PH6661	SC07	FET
PH13002	SC06	SP
PH13003	SC06	SP
PHSD51	S2a	R
PKB3001U	SC15	M
PKB3003U	SC15	M
PKB3005U	SC15	M
PKB12005U	SC15	M
PKB20010U	SC15	M
PKB23001U	SC15	M
PKB23003U	SC15	M
PKB23005U	SC15	M
PKB25006T	SC15	M
PKB32001U	SC15	M
PKB32003U	SC15	M
PKB32005U	SC15	M
PLED-G313A	S8a	LED
PLED-G313N	S8a	LED
PLED-G314A	S8a	LED
PLED-G314N	S8a	LED
PLED-G511C	S8a	LED
PLED-G513C	S8a	LED
PLED-G513M	S8a	LED
PLED-G514B	S8a	LED
PLED-G514M	S8a	LED
PLED-G544KL	S8a	LED
PLED-G544LL	S8a	LED
PLED-GR14E	S8a	LED
PLED-GR14F	S8a	LED
PLED-GR14G	S8a	LED
PLED-GR44DL	S8a	LED
PLED-H313A	S8a	LED
PLED-H314A	S8a	LED
PLED-H511C	S8a	LED
PLED-H514B	S8a	LED
PLED-H544KL	S8a	LED
PLED-H544LL	S8a	LED
PLED-HR14E	S8a	LED
PLED-HR14F	S8a	LED
PLED-HR14G	S8a	LED
PLED-HR44DL	S8a	LED
PLED-0313N	S8a	LED
PLED-0314N	S8a	LED
PLED-0513M	S8a	LED
PLED-0514M	S8a	LED
PLED-P313N	S8a	LED
PLED-P314N	S8a	LED
PLED-P513M	S8a	LED
PLED-P514M	S8a	LED
PLED-T512B	S8a	LED
PLED-TR12E	S8a	LED
PLED-TR12F	S8a	LED
PLED-TR12G	S8a	LED
PLED-TR42DL	S8a	LED
PLED-Y313A	S8a	LED
PLED-Y313N	S8a	LED
PLED-Y314A	S8a	LED
PLED-Y314N	S8a	LED
PLED-Y511C	S8a	LED
PLED-Y513C	S8a	LED
PLED-Y513M	S8a	LED
PLED-Y514B	S8a	LED
PLED-Y514M	S8a	LED
PLED-Y544KL	S8a	LED
PLED-Y544LL	S8a	LED
PLED-YR14E	S8a	LED
PLED-YR14F	S8a	LED
PLED-YR14G	S8a	LED
PLED-YR44DL	S8a	LED
PMBD914	SC01	SD
PMBD2835	SC01	SD
PMBD2836	SC01	SD
PMBD2837	SC01	SD
PMBD2838	SC01	SD
PMBD6050	SC01	SD
PMBD6100	SC01	SD
PMBD7000	SC01	SD
PMBF170	SC07/10	FET/Mm
PMBF4391	SC07/10	FET/Mm
PMBF4392	SC07/10	FET/Mm
PMBF4393	SC07/10	FET/Mm
PMBFJ174	SC07/10	FET/Mm
PMBJF175	SC07/10	FET/Mm
PMBJF176	SC07/10	FET/Mm
PMBJF177	SC07/10	FET/Mm
PMBT2222	SC10	Mm
PMBT2222A	SC10	Mm
PMBT2369	SC10	Mm
PMBT2907	SC10	Mm
PMBT2907A	SC10	Mm
PMBT3903	SC10	Mm
PMBT3904	SC10	Mm
PMBT3906	SC10	Mm
PMBT4401	SC10	Mm
PMBT4403	SC10	Mm
PMBT5088	SC10	Mm
PMBT5401	SC10	Mm
PMBT5550	SC10	Mm
PMBT5551	SC10	Mm
PMBT6428	SC10	Mm
PMBT6429	SC10	Mm
PMBTA05	SC10	Mm
PMBTA06	SC10	Mm
PMBTA13	SC10	Mm
PMBTA14	SC10	Mm
PMBTA42	SC10	Mm
PMBTA43	SC10	Mm
PMBTA55	SC10	Mm
PMBTA56	SC10	Mm
PMBTA63	SC10	Mm
PMBTA64	SC10	Mm
PMBTA92	SC10	Mm
PMBTA93	SC10	Mm
PMBZ5226	SC01	SD

type no.	book	section
PMLL4148	SC01/10	SD/Mm
PMLL4150	SC01/10	SD/Mm
PMLL4151	SC01/10	SD/Mm
PMLL4153	SC01/10	SD/Mm
PMLL4446	SC01/10	SD/Mm
PMLL4448	SC01/10	SD/Mm
PMLL5225B		
to	SC01/10	SD/Mm
PMLL5267B		
PN2222	SC04	Sm
PN2222A	SC04	Sm
PN2369	SC04	Sm
PN2369A	SC04	Sm
PN2907	SC04	Sm
PN2907A	SC04	Sm
PN3439	SC04	Sm
PN3440	SC04	Sm
PN4391	SC07	FET
PN4392	SC07	FET
PN4393	SC07	FET
PN5415	SC04	Sm
PN5416	SC04	Sm
PO44	SC12	PhC
PO44A	SC12	PhC
PPC5001T	SC15	M
PQC5001T	SC15	M
PTB23001X	SC15	M
PTB23003X	SC15	M
PTB23005X	SC15	M
PTB32001X	SC15	M
PTB32003X	SC15	M
PTB32005X	SC15	M
PTB42001X	SC15	M
PTB42002X	SC15	M
PTB42003X	SC15	M
PV3742B4X	SC15	M
PVB42004X	SC15	M
PXT2222	SC10	Mm
PXT2222A	SC10	Mm
PXT2907	SC10	Mm
PXT2907A	SC10	Mm
PXT3904	SC10	Mm
PXT3906	SC10	Mm
PXT4401	SC10	Mm
PXT4403	SC10	Mm
PXTA14	SC10	Mm
PXTA27	SC10	Mm
PXTA64	SC10	Mm
PXTA77	SC10	Mm
PZ1418B15U	SC15	M
PZ1418B30U	SC15	M
PZ1721B12U	SC15	M
PZ1721B25U	SC15	M
PZ2024B10U	SC15	M
PZ2024B20U	SC15	M
PZ2327B15U	SC15	M
PZB16035U	SC15	M
PZB16040U	SC15	M
PZB27020U	SC15	M
PZT2222	SC10	Mm
PZT2222A	SC10	Mm
PZT2907	SC10	Mm
PZT2907A	SC10	Mm
PZT3904	SC10	Mm
PZT3906	SC10	Mm
PZTA13	SC10	Mm
PZTA14	SC10	Mm
PZTA42	SC10	Mm
PZTA43	SC10	Mm
PZTA63	SC10	Mm
PZTA64	SC10	Mm
PZTA92	SC10	Mm
PZTA93	SC10	Mm
RPY97	SC12	I
RPY100	SC12	I
RPY101	SC12	I
RPY102	SC12	I
RPY103	SC12	I
RPY107	SC12	I
RPY109	SC12	I
RV2833B5X	SC15	M
RV3135B5X	SC15	M
RX1011B250Y	SC15	M
RX1011B350Y	SC15	M
RX1214B150Y	SC15	M
RX1214B300Y	SC15	M
RX2731B90W	SC15	M
RX3034B70W	SC15	M
RXB12350Y	SC15	M
RZ1214B35Y	SC15	M
RZ1214B65Y	SC15	M
RZ1214B125Y	SC15	M
RZ1214B150Y	SC15	M
RZ2731B45W	SC15	M
RZ2731B60W	SC15	M
RZ2833B15W	SC15	M
RZ2833B30W	SC15	M
RZ2833B45W	SC15	M
RZ2833B60W	SC15	M
RZ3135B15W	SC15	M
RZ3135B30W	SC15	M
RZ3135B40W	SC15	M
RZ3135B50W	SC15	M
RZB12050Y	SC15	M
RZB12100Y	SC15	M
RZB12250Y	SC15	M
SL5500	SC12	PhC
SL5501	SC12	PhC
SL5502R	SC12	PhC
SL5504	SC12	PhC
SL5504S	SC12	PhC
SL5505S	SC12	PhC
SL5511	SC12	PhC
TIP29*	SC05	P
TIP30*	SC05	P
TIP31*	SC05	P
TIP32*	SC05	P
TIP33*	SC05	P
TIP34*	SC05	P
TIP41*	SC05	P
TIP42*	SC05	P
TIP47	SC06	P
TIP48	SC06	P
TIP49	SC06	P
TIP50	SC06	P
TIP110	SC05	P
TIP111	SC05	P
TIP112	SC05	P
TIP115	SC05	P
TIP116	SC05	P
TIP117	SC05	P
TIP120	SC05	P
TIP121	SC05	P
TIP122	SC05	P
TIP125	SC05	P

type no.	book	section
TIP126	SC05	P
TIP127	SC05	P
TIP130	SC05	P
TIP131	SC05	P
TIP132	SC05	P
TIP135	SC05	P
TIP136	SC05	P
TIP137	SC05	P
TIP140	SC05	P
TIP141	SC05	P
TIP142	SC05	P
TIP145	SC05	P
TIP146	SC05	P
TIP147	SC05	P
TIP2955	SC05	P
TIP2955T	SC05	P
TIP3055	SC05	P
TIP3055T	SC05	P
1N821	SC01	Vrf
1N821A	SC01	Vrf
1N823	SC01	Vrf
1N823A	SC01	Vrf
1N825	SC01	Vrf
1N825A	SC01	Vrf
1N827	SC01	Vrf
1N827A	SC01	Vrf
1N829	SC01	Vrf
1N829A	SC01	Vrf
1N914	SC01	SD
1N916	SC01	SD
1N3879	S2a	R
1N3880	S2a	R
1N3881	S2a	R
1N3882	S2a	R
1N3883	S2a	R
1N3889	S2a	R
1N3890	S2a	R
1N3891	S2a	R
1N3892	S2a	R
1N3893	S2a	R
1N3909	S2a	R
1N3910	S2a	R
1N3911	S2a	R
1N3912	S2a	R
1N3913	S2a	R
1N4001D	SC01	R
1N4002D	SC01	R
1N4003D	SC01	R
1N4004D	SC01	R
1N4005D	SC01	R
1N4006D	SC01	R
1N4007D	SC01	R
1N4001G	SC01	R
1N4002G	SC01	R
1N4003G	SC01	R
1N4004G	SC01	R
1N4005G	SC01	R
1N4006G	SC01	R
1N4007G	SC01	R
1N4148	SC01	SD
1N4150	SC01	SD
1N4151	SC01	SD
1N4153	SC01	SD
1N4446	SC01	SD
1N4448	SC01	SD
1N4531	SC01	SD
1N4532	SC01	SD
1N4933	SC01	R
1N5059	SC01	R
1N5060	SC01	R
1N5061	SC01	R
1N5062	SC01	R
1N5225 to	SC01	R
1N5267B	SC01	R
2N918	SC14	WBT
2N930	SC04	Sm
2N1613	SC04	Sm
2N1711	SC04	Sm
2N1893	SC04	Sm
2N2219	SC04	Sm
2N2219A	SC04	Sm
2N2222	SC04	Sm
2N2222A	SC04	Sm
2N2297	SC04	Sm
2N2369	SC04	Sm
2N2369A	SC04	Sm
2N2483	SC04	Sm
2N2484	SC04	Sm
2N2904	SC04	Sm
2N2904A	SC04	Sm
2N2905	SC04	Sm
2N2905A	SC04	Sm
2N2906	SC04	Sm
2N2906A	SC04	Sm
2N2907	SC04	Sm
2N2907A	SC04	Sm
2N3019	SC04	Sm
2N3020	SC04	Sm
2N3053	SC04	Sm
2N3375	SC08	RFP
2N3439	SC04	Sm
2N3440	SC04	Sm
2N3553	SC08	RFP
2N3632	SC08	RFP
2N3822	SC07	FET
2N3823	SC07	FET
2N3866	SC08	RFP
2N3903	SC04	Sm
2N3904	SC04	Sm
2N3905	SC04	Sm
2N3906	SC04	Sm
2N3924	SC08	RFP
2N3926	SC08	RFP
2N3927	SC08	RFP
2N3966	SC07	FET
2N4030	SC04	Sm
2N4031	SC04	Sm
2N4032	SC04	Sm
2N4033	SC04	Sm
2N4036	SC04	Sm
2N4091	SC07	FET
2N4092	SC07	FET
2N4093	SC07	FET
2N4123	SC04	Sm
2N4124	SC04	Sm
2N4125	SC04	Sm
2N4126	SC04	Sm
2N4391	SC07	FET
2N4392	SC07	FET
2N4393	SC07	FET
2N4400	SC04	Sm
2N4401	SC04	Sm
2N4402	SC04	Sm
2N4403	SC04	Sm
2N4427	SC08	RFP

type no.	book	section
2N4856	SC07	FET
2N4857	SC07	FET
2N4858	SC07	FET
2N4859	SC07	FET
2N4860	SC07	FET
2N4861	SC07	FET
2N5086	SC04	Sm
2N5087	SC04	Sm
2N5088	SC04	Sm
2N5400	SC04	Sm
2N5401	SC04	Sm
2N5415	SC04	Sm
2N5416	SC04	Sm
2N5550	SC04	Sm
2N5551	SC04	Sm
2N6659	SC07	FET
2N6660	SC07	FET
2N6661	SC07	FET
2PA733	SC04	Sm
2PA1015/L	SC04	Sm
2PC945	SC04	Sm
2PC1815/L	SC04	Sm
4N25	SC12	PhC
4N25A	SC12	PhC
4N26	SC12	PhC
4N27	SC12	PhC
4N28	SC12	PhC
4N35	SC12	PhC
4N36	SC12	PhC
4N37	SC12	PhC
4N38	SC12	PhC
4N38A	SC12	PhC
56201d	SC06	A
56201j	SC06	A
56245	SC04/14	A
56246	SC04/14	A
56261a	SC06	A
56264	S2a/b	A
56295	S2a/b	A
56326	SC06	A
56339	SC06	A
56352	SC06	A
56353	SC06	A
56354	SC06	A
56359b	S2/4	A
56359c	S2/4	A
56359d	S2/4	A
56360a	S2/4	A
56363	S2/4	A
56364	S2/4	A
56367	S2/4	A
56368b	S2/4	A
56368c	S2/4	A
56369	S2/4	A
56378	S2/4	A
56379	S2/4	A
56387a	SC06	A
56387b	SC06	A
56397	SC01	A

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

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Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08**	**RF power transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display components**
T16	**DC02**	**Monochrome monitor tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers, encoders and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	**Power tubes for RF heating and communications**
T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
T3	**PC01****	**High-power klystrons**
T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
T6	**PC03****	**Geiger-Müller tubes**
T9	**PC04****	**Photo and electron multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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